CURRENT MIRROR AND CURRENT LIMITER BASED HIGH PERFORMANCE VOLTAGE LEVEL SHIFTER

Abstract

The paper presents a high-performance voltage level shifter design based on a current mirror and current limiter circuit. The proposed circuit can shift a low voltage level signal to a high voltage level signal with low power consumption and high-speed operation. The current mirror circuit is used to generate a reference current, which is then compared with the input current using a current limiter cir- cuit to control the output voltage. The proposed design achieves a wide voltage range and a high output impedance, making it suitable for various applications, including low-power and high-speed applications. Simulation results demonstrate the effectiveness of the proposed design in terms of low power consumption, high speed, and excellent performance. The proposed circuit can be implemented in various technology nodes, making it a promising solution for future integrated circuits.

Keywords: Current limiter, Delay, IoT application, Level shifter, Power consumption.

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I. INTRODUCTION

A voltage level shifter is an essential component in elec- tronic circuits that enables the translation of signals between different voltage domains. The current mirror and current limiter based voltage level shifter is a high-performance solution that provides accurate and reliable voltage transla- tion with minimal power consumption.

The current mirror is a circuit that produces an output current that is proportional to the input current. In a current mirror-based voltage level shifter, the input voltage is con- verted to a current using a simple transconductance amplifi- er, and this current is mirrored to the output stage to gener- ate the desired output voltage. The current limiter, on the other hand, is a circuit that limits the maximum current that can flow through a device. In a currentlimiter-based voltage level shifter, the input current is first limited using a current limiter, and then the limited current is mirrored to the output stage to produce the desired output voltage.

The combination of these two techniques in a voltage level shifter results in a circuit that is capable of translating signals between voltage domains with high accuracy and low power consumption. This makes it an ideal solution for applications where signal integrity and power efficiency are critical, such as in portable devices, data acquisition sys- tems, and sensor networks.

II. EXISTING SYSTEM

The most popular current-limiters are set up with a voltage drop from supply rails that are too high for their low-voltage supply. The better match is the design with a reduced voltage drop. When internal current-limiters are required for the supply voltages, they are frequently made utilizing current sensors, control circuits, and pass transistors. Simple low-value resistors constructed with MOS transistors serve as the current sensors.

The pull-up network's current contention is lessened by the circuit current limiters MN1 and MN2 MOS transistors. MOS transistor MN5 turns on pull-down when the voltage input VIN is transitioning from voltage low to voltage high.

With full swing output voltage VOUT, this will invert the MN8-MP4 inverter's output. The potential short circuit current at the output inverter may increase at the VIN high to minimal voltage change. MN3-MN4 created a new pair of limiters to avoid their previous pair.

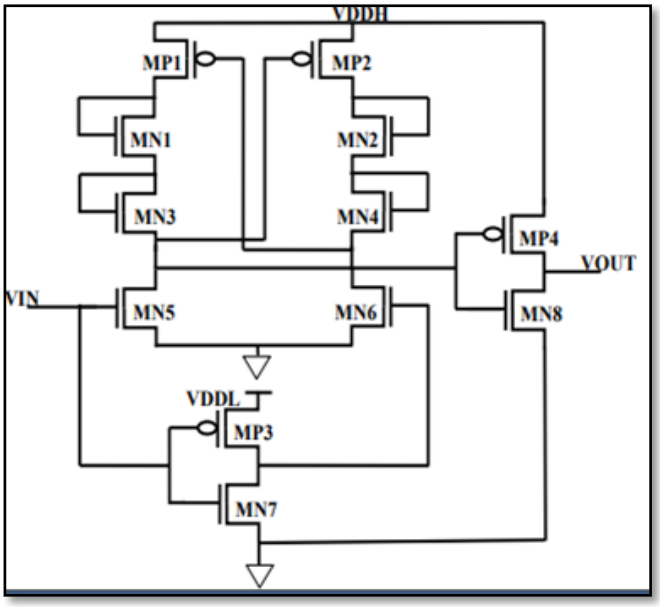

Figure 1: DCVS Level Shifter

When VIN is logic '1', which is as little as 0.15V, MOS transistor MN5 switches ON and VDDL inverter MP3-MN7 generates a strong logic '0', turning MN6 OFF.

The driving inverter MP4-MN8 generates the strong logic '1', or 1.25V, when MN6 is ON, by pulling up the MP4 ON.At the point when the voltage swing is low in the primary transformation stage and the current is restricted through the ongoing limiters MN1-MN2 and MN3-MN4 the better power utilization and defer might accomplish.

Disadvantages

- High delay
- High power consumption

III. PROPOSED METHOD

The proposed level shifter circuit consists of two voltage levels one is low voltage level (VDDL) another high voltage level (VDDH), here we are able to achieve the better power consumption and delay when compared to existing voltage level shifter.

The proposed level shifter is designed by using current mirror and current limiter circuit. Current limiter circuit is used to limit the current flow and avoid the short circuit path.

The simple current mirror circuit is designed by connecting the drain terminal of PMOS or NMOS to the gate terminal of the same transistor.

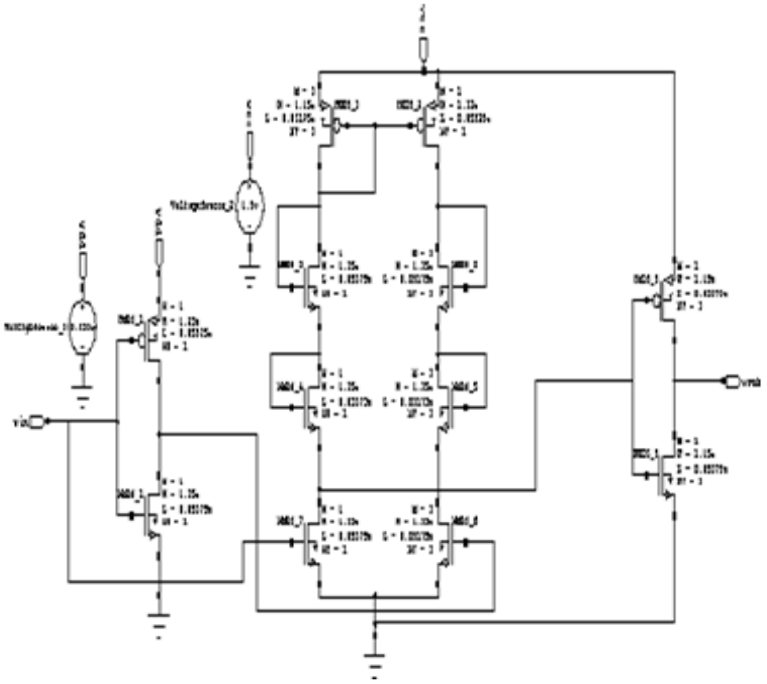

Figure 2: Proposed Method

The ongoing in one semiconductor will precisely reflect that of the second, it are precisely matched to expect that the two semiconductors. It will give the steady current.

Here input supply voltage in the range of 0.29v to 0.4 v can able to achieve up to the high voltage level 1.5v.

When VIN is logic ‘1’, then NM7 transistor is on NM6 isoff .

Here the current limiter is avoid the short circuit path and power consumption of the level shifter and delay can be achieved.

IV. LITERATURE SURVEY

The LS "A Super Low Voltage-Level Shifter Utilizing Re-vised Wilson Current Mirror for Quick and Energy-Proficient Wide-Reach Voltage Change from Sub-Limit to I/O Voltage" is a Wilson current mirror model. Wilson current mirror includes an information-controlled diode and criticism control makes LS achieves little engendering delay and less power scattering for wide voltage change from underneath edge to I/O range. It moreover uses "Blended gadget and Inverses restricted width gadget" measuring to work on the general postponement and power.

Summary: From this article, sizing is used to improve the overall delay and power. The LS named "Low-Power Level Shifter for Multi Supply Voltage Plans is a changed DCVSL design" is the DCVSL model. In this paper novel, low-power LS for energetic voltage moving from the close or sub-limit to the above edge voltage is proposed. The plan takes advantage of plan procedures to restrict energy and static power. Due to these features,

the proposed LS display lower static power and energy.

Summary: From this article, Level shifter exhibit lowerstatic power and energy.

V. RESULTS AND DISCUSSION

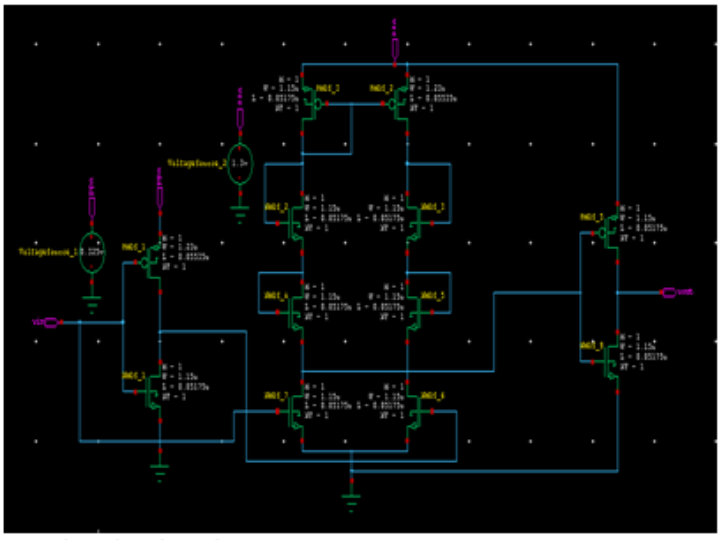

Figure 3: Schematic of proposed Schmitt trigger

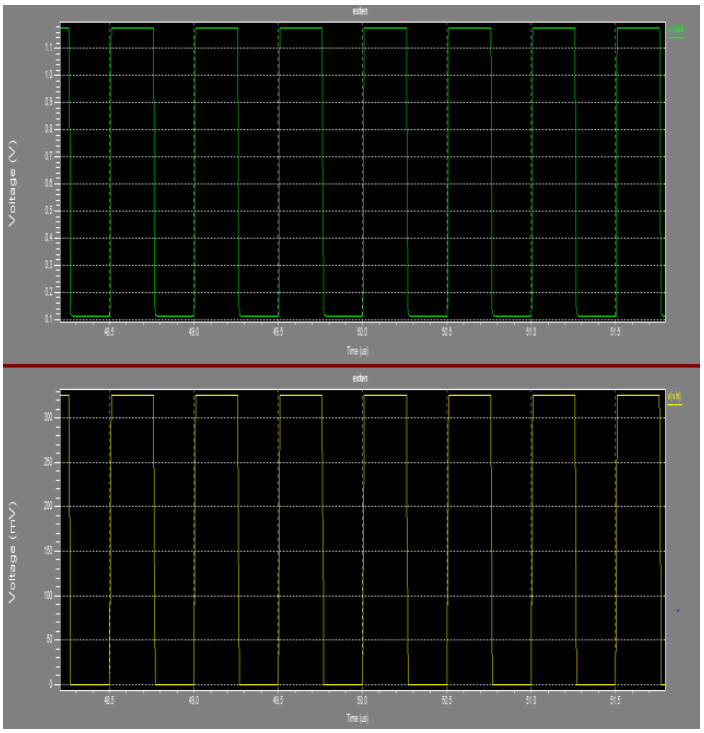

Figure 4: Simulated output of differential pair of the proposedSchmitt trigger

Table 1: Comparison between Existing andProposed Level Shifter

PARAMETER	EXISTING METHOD	PROPOSED METHOD
Power	6.2315	5.991
Dealy	2.9526	0.5466
Area	12	12

VI. CONCLUSION

The proposed current mirror and current limiter based superior execution voltage level shifter circuit is planned by utilizing 45nm CMOS innovation to play out the voltage level moving from 0.3V to 1.4V. The outcomes demonstrate that the favorable to presented circuit serenely moves at low power utilization. The proposed plan can be as powerful in light of the wide transformation range as well as meeting every one of the prerequisites of IOT necessities.

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