INTEGRATED CIRCUITS FABRICATION TECHNIQUES FOR C-MOS, N-MOS AND BJT

Abstract

Integrated Circuit designs will be realised in one of a number of possible fabrication processes. The circuit fabricated on a die will then be packaged within a suitable protective housing. The particular fabrication process to use will be dependent on a number of issues including cost, availability, experience in the use of, and circuit component capabilities. Complex processes and technology utilizing minute dimensions are essential to the fabrication of today's high density integrated circuits. The key unit processes for circuit fabrication outlined within this paper are chemical vapor deposition, oxidation, diffusion and ion implantation, metallization and lithography. The parallel advances of these processes have led to a new era of very large scale integrated (VLSI) circuits with low micrometer to submicron features that result in denser, faster and more complex devices. The most critical advances, however, have been in the areas of lithography and etching, where electron-beam systems, along with plasma-assisted etching techniques, have enabled further miniaturization. New materials have been developed, including the low resistivity silicdes. Packaging advances also translate into major production cost savings. Finally, the interaction of computer aided design, process simulation, production/process control, in-process measurement, characterization and final testing play a critical role in VLSI fabrication technology.

Keywords: VLSI Technology, CMOS IC Fabrication, NMOS IC Fabrication, BJT IC Fabrication, Fabrication, Etching, Diffusion Metallization

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I. INTRODUCTION

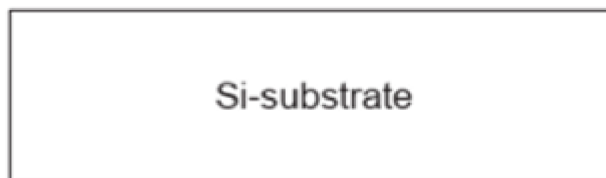
The Integrated Circuits are the set of digital electronics circuits set up on the small electronic chip. Big numbers of devices, such as MOSFETs (metallic Oxide Semiconductor field effect Transistor), transistors, microcontrollers, computer processors, and so on, are created with the assist of the fabrication method. The most favoured materials within the semiconductor industry for fabrication are silicon and germanium because of their solid structure. Other materials favoured in fabrication industries are carbon steel, silver, aluminium, magnesium, copper, wood, thermoplastics, resins, and so forth.

Fabrication is the procedure of building a commercial product. We can also define it as a fixed of techniques to fabricate a digital tool or product. For instance, silicon semiconductor chips, etc. In the case of metals, fabrication is a method used to transform the raw substances into the furnished product.

II. NMOS IC FABRICATION

The first technology we will discussing is the n channel metal oxide semiconductor i.e. NMOS. It has three terminals which includes source, drain and gate. The impurities that will be doped in the NMOS will be pentavalent in nature (five valence electron), for eg. Boron and antimony. As the name suggest, a n-type channel is created on a p-type substrate. The NMOS fabrication procedure is the least complex because it requires the least number of lithography levels. Furthermore, the fundamental aspects of the NMOS technology are also important for the complementary metal - oxide - semiconductor (CMOS) technology. The NMOS fabrication steps are discussed below:

Step 1: Substrate Formation: The first step to begin with is to create a p - type substrate. This p-type substrate includes impurities (trivalent in nature) such as boron (conc. level up to $1016/cm^3$). A pure skinny film of the Silicon wafer is chosen on the p type impurities as crystals. The diameter of the wafer is selected to be about 0.15m or 150mm. The most suitable wafer material is silicon because it is clean and high-quality semiconductor material and generally preferred for fabrication.



Step 2: Growth of SiO_2 layer: A SiO2 layer is grown on the surface of silicon wafer. This SiO2 layer acts as a barrier to the dopant throughout the processing and acts as an insulating substrate on to which various layers might be deposited and patterned. The thickness of this layer is generally around 0.000001m, which is very small.

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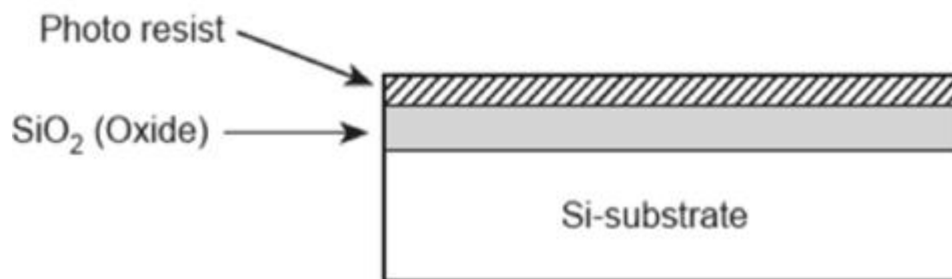
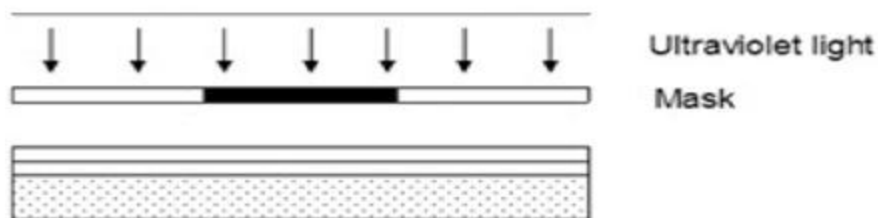
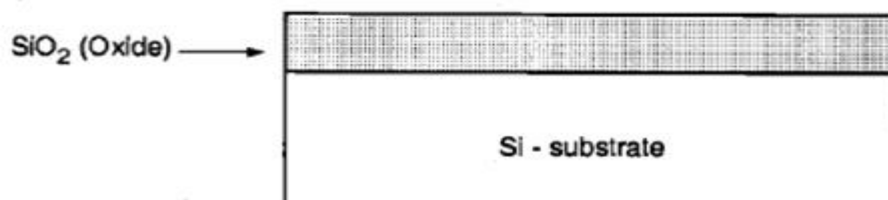
Step 3: Coating of photoresist material on SiO_2 layer: Now, on the surface of SiO_2 layer, a layer of photoresist material is coated. This Photoresist material layer gets deposited onto the wafer and spread uniformly to obtain required thickness.



Step 4: Process of Photolithography: The photoresist layer deposited in the previous step is now exposed to ultraviolet radiation. For this a mask is created. Mask determines the regions through which the diffusion will takes place. The mask will split into two regions, one which is covered and another which is exposed to UV radiation. The areas which get exposed by UV radiation becomes polymerized (hardened). The areas where diffusion process will take place are guarded by the mask.



Step 5: Etching : The unexposed areas are removed from the surface and the regions are etched together to form a clean wafer surface as shown below:



Step 6: Growth of SiO_2 and Polysilicon layer: Now another layer of SiO_2 of 0.2 pm thickness is deposited over the entire surface. Then a layer of polysilicon is grown above the oxide layer. The polysilicon layer is deposited by CVD method, this forms gate structure of NMOS.

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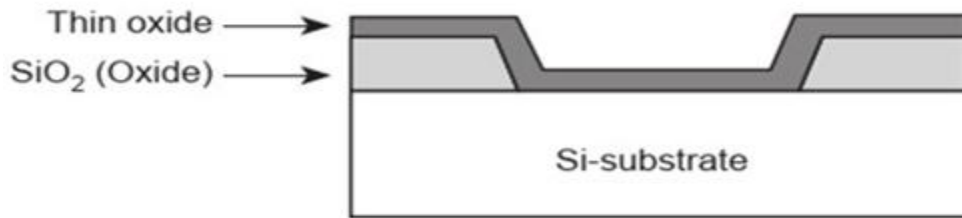
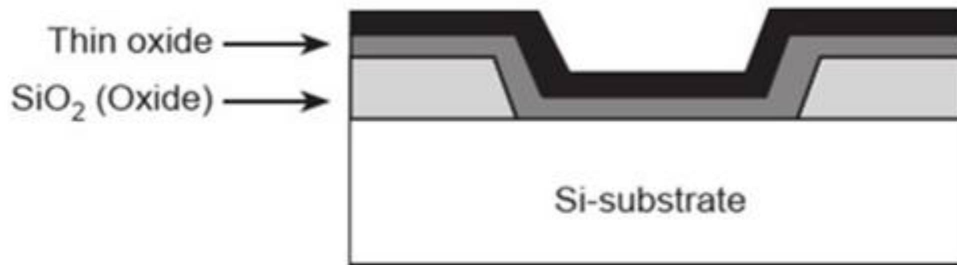
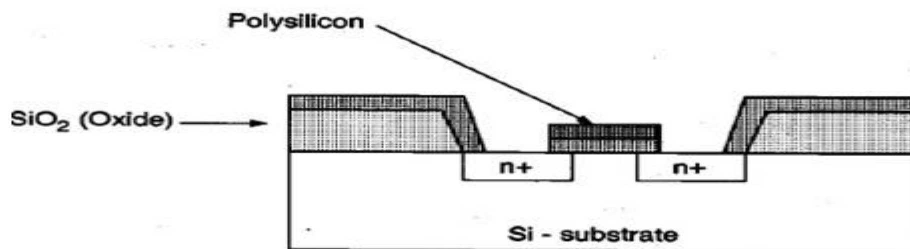
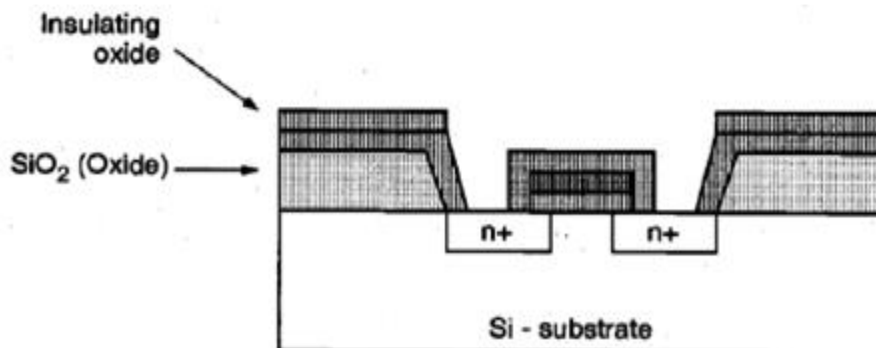




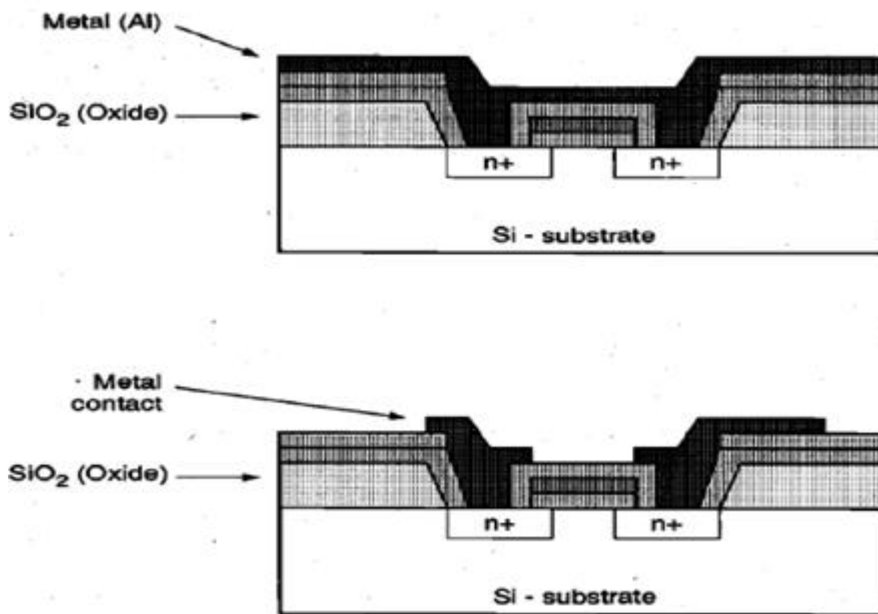
Step 7: Diffusion Proces : The oxide and the polysilicon layer on the surface of the wafer is etched and n-type impurities are introduced by the diffusion process into the specified exposed area. The n-channels at the source and drain terminals are established.



Step 8: SiO_2 and photoresist is again deposited on the source and drain terminals: The process in step 6 is again repeated to protect the source and drain terminal. The oxide layer is etched from the surface of the wafer so that the two terminals can be created. The SiO2 and photoresists are deposited and photolithography process is repeated. The contact holes area are left exposed and space for connection are left behind.



Step 9: Deposition of Metal layer: This is the last step of the NMOS fabrication process. A layer of evaporated aluminium is spreaded on the surface of wafer including the contact holes. This aluminium layer is around 1um thick. The metallic layer is again masked and etched (photolithography) to form the desired interconnection pattern.

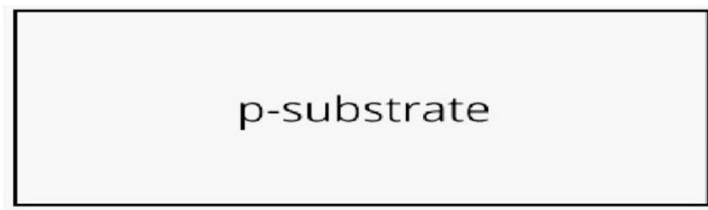


III. CMOS IC FABRICATION

CMOS stands for Complementary Metal Oxide Semiconductor and this is the next technology whose fabrication process will be studied in this section. It is a combination of NMOS and PMOS which are fabricated in different ways. In this a PMOS is produced by placing it in the n-well which has a p-type channel. And NMOS is similarly created as discussed in NMOS fabrication section.

The various steps involving CMOS fabrication process is discussed below:

1. **Wafer Selection:** We select a silicon wafer in which we will dope p-type impurities and these impurities are trivalent in nature and so the doped wafer formed will be a p-type substrate.



2. **Growth of SiO_2 layer:** A SiO_2 layer is grown on the surface of silicon wafer that protects the substrate as discussed in the step 2 of NMOS fabrication process section.

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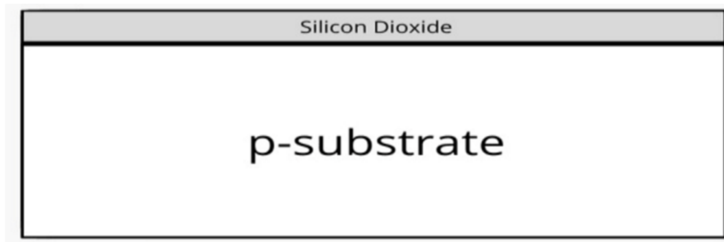
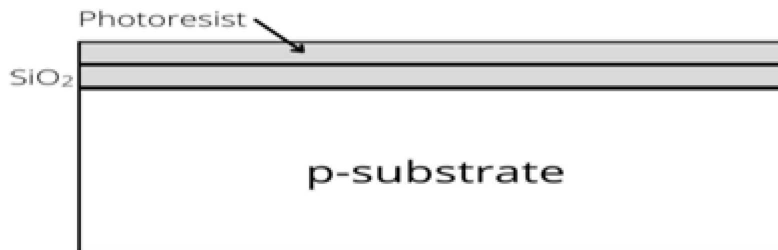
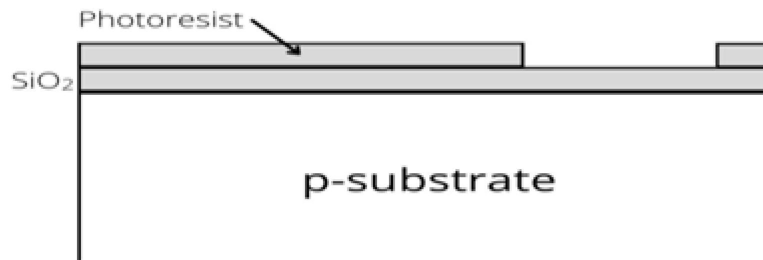


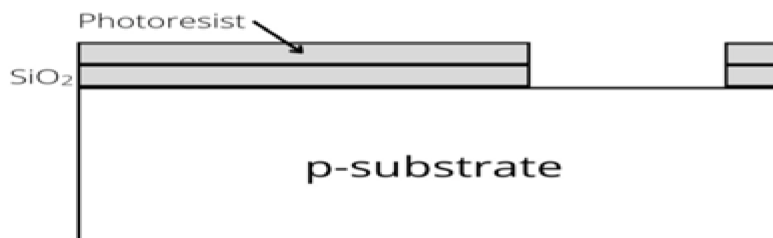
3. **Coating of photoresist material on SiO_2 layer:** In this, on the surface of SiO_2 layer, photoresist material is coated. It will help us in forming the n-well on the p-type substrate.



4. **Formation of N-well:** At this stage, the photoresist material is highly insoluble so we place a mask over the substrate covered by SiO_2 and photoresist layer. Through this n-well mask uv light is exposed (photolithography).



5. **Oxide etching:** As we saw in the previous figure the right side of the wafer is not covered by the photoresist. Since we have to form a n-well in this part we will etch the oxide layer using Hydrofluoric acid. So, along with the oxide layer the remaining photoresist will also be etched. Now, our silicon wafer is ready to get dopped in the n-well area.



6. **Diffusion in N-Well:** Now, we will use the diffusion process to form a n-well on the right side of the wafer. Using this diffusion process impurities will be added to the right part. Ion implantation can also be used to create the n-well.

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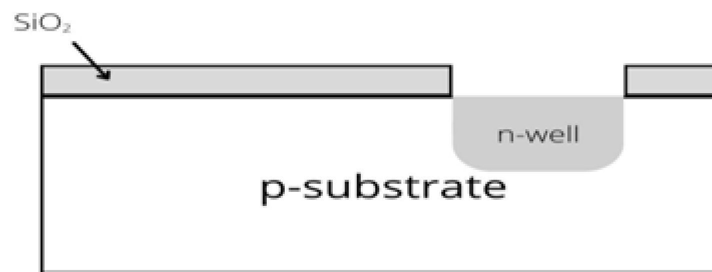
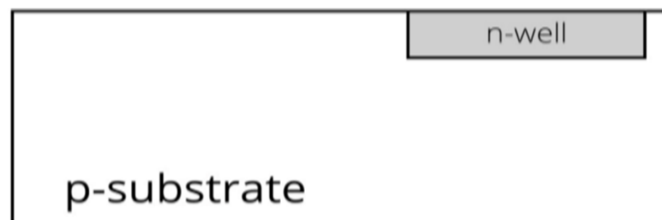
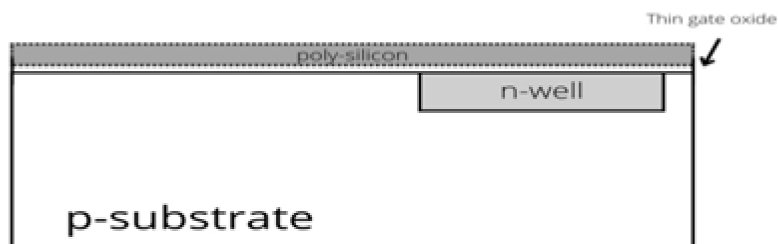


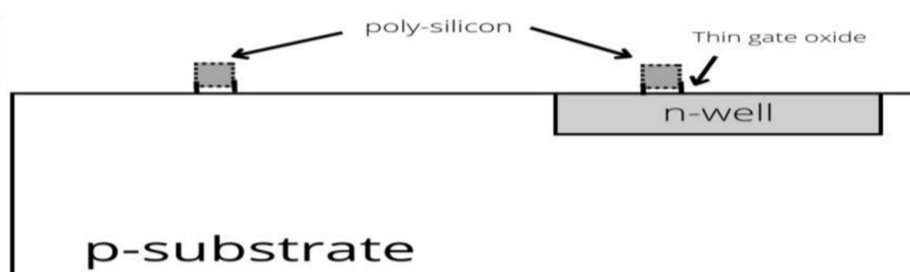
7. **Removal of SiO_2:** The remaining oxide on the surface of the wafer is etched with the help of Hydrofluoric acid (photolithography process is repeated).



8. **Gate formation:** In the previous step, we removed the remaining oxide layer to create a gate junction. A polysilicon layer is added to the surface of the wafer by using CVD process to form a gate structure. This layer of polysilicon is heavily doped over a thin gate oxide.

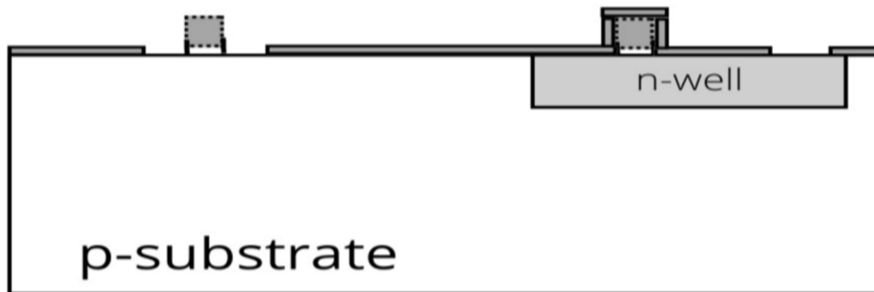


9. **Patterning of poly silicon layer:** As we know CMOS is a combination of PMOS and NMOS, so we need two separate gate terminals. To obtain these two separate gate terminals photolithography process is repeated. The two gate terminals which are formed are shown below in the figure.

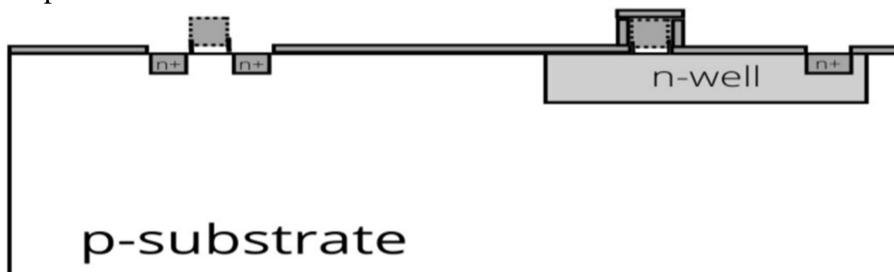


10. **Diffusion pattern:** The entire surface of the wafer is covered by a protective thin layer of the oxide. The purpose of this thin layer is to protect the two gate terminals.

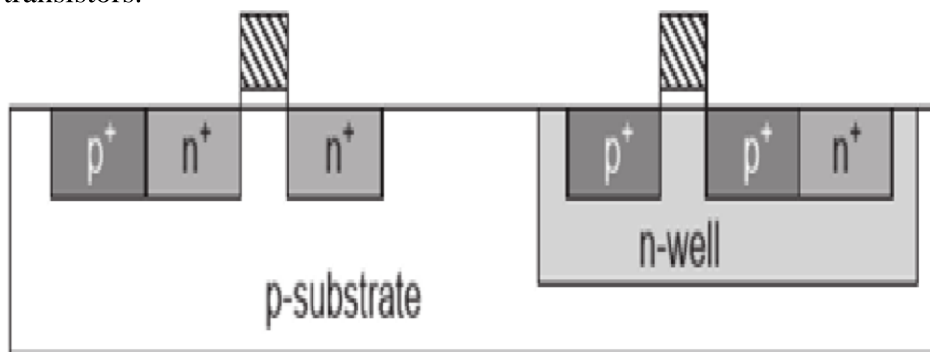
11. **Formation of source and drain:** To form the source and drain terminals the protective oxide is removed using photolithography process. After the photolithography process is completed two vacant areas are created.



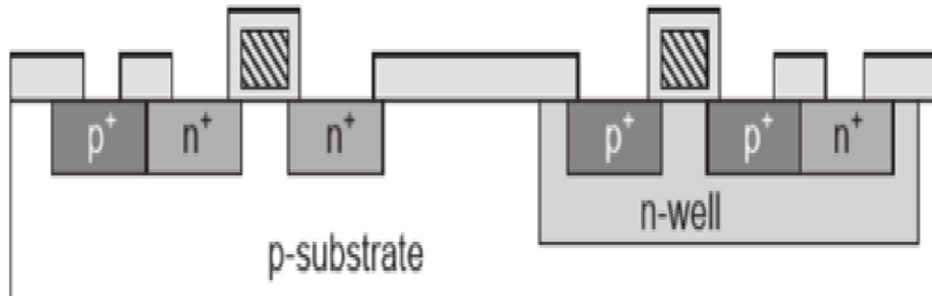
12. **N-diffusion regions:** The two vacant areas mentioned above include two source terminals and two drain terminals on each side. The N-diffusion regions are produced either by diffusion or ion implantation process. Now, the source and drain terminals are automatically formed on the adjacent sides of the gate terminals. During this process the wafer is heated to a high temperature to create a n-well regions through the diffusion process.



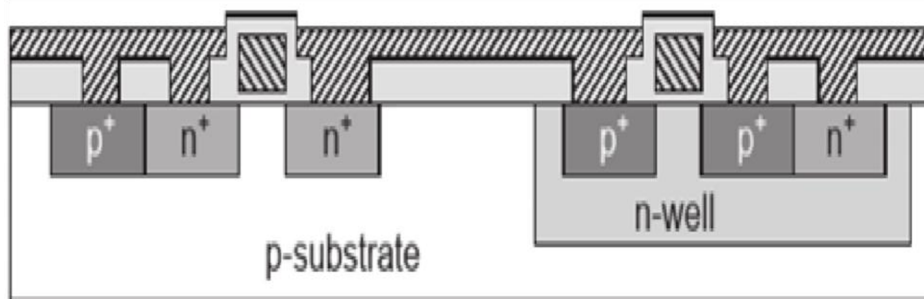
13. **P-diffusion:** In the earlier step, the n^+ regions are already created and since NMOS has n^+ source and drain regions while the PMOS has p^+ regions. Now, the p^+ diffusion mask is used (photolithography) which completes our formation of all the active regions of the MOS transistors.



14. **Insulating field oxide deposition:** In order to insulate the wafer, the field oxide SiO_2 is deposited on the surface. Now, we will etch the oxide where contact cuts are needed.



15. **Metal formation:** Now, evaporated aluminium is coated on the surface of the wafer. This forms a metal layer on the surface of the wafer. Now, patterning (photolithography) is done to obtain the contact holes.



The formation of CMOS is completed.

IV. BJT FABRICATION

Bipolar transistor fabrication and their shape has come a protracted manner since the first transistors were made. Today's transistors are made suing sophisticated tactics and the structure of transistor permits them to have very high stage of performance. The unique transistor made by Bardeen, Brattain and Shockley consisted of two very narrowly spaced contacts on a germanium base. The shape of this transistor consisted of two-point contacts on a base of germanium. These days the transistors are made by using various methods and of different structures. They might be diffused, epitaxially grown or they will use a mesa production. In essence a transistor consists of an area of both p -type of n type semiconductor sandwiched among areas of oppositely doped silicon. As such gadgets can be either a p-n-p or an n-p-n configuration.

There are 3 terminals, namely the emitter, base, and the collector. The base is the only within the centre and it's far bounded via the emitter and collector. Of the two outer the collector is frequently made large as that is in which most of the heat is dissipated.
The base derives its name from the first point attached transistors in which the centre connection also fashioned the mechanical "base" for the structure. It's important that this region need to be as skinny if high stages of modern advantage are to be executed. Often it

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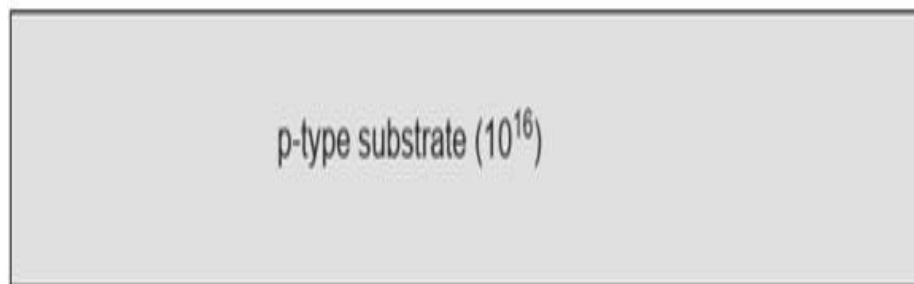
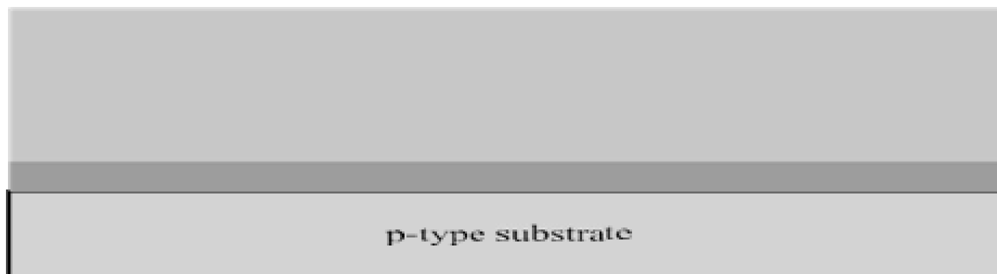
can be handiest for about 1 micro meter throughout. An emitter is where the current is emitted, and the collector is wherein they're collected. BJT Fabrication steps are as follows:

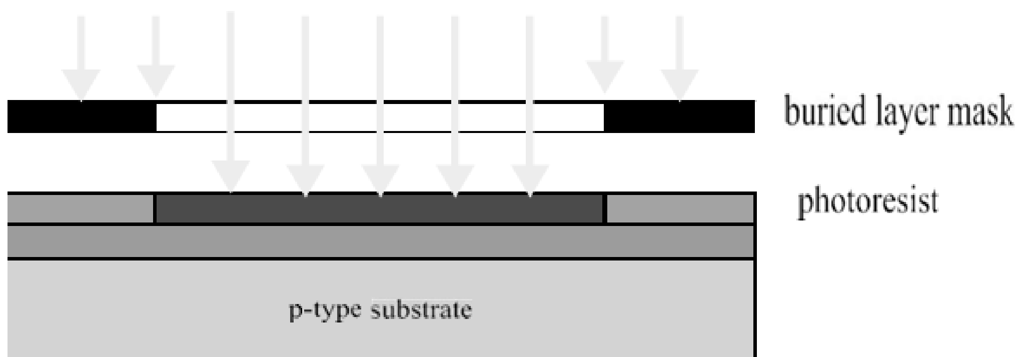
1. **The BJT fabrication - starting fabric:** The starting material for a vertical n-p-n arrangement is p-type substrate doped at 10^s16 /cm3 or less.



2. **The BJT fabrication - first oxide deposition:** Using a Chemical Vapour Deposition (CVD), oxide is deposited at the surface of wafer.



3. **Patterning of the first oxide:** Photoresist spun on the top of the oxide and is exposed using the buried layer mask. The BL mask is commonly generated mechanically from other masks.



4. **Etching of the first oxide:** Using wet etching process, a window which is corresponding to the buried layer mask is opened in the oxide.

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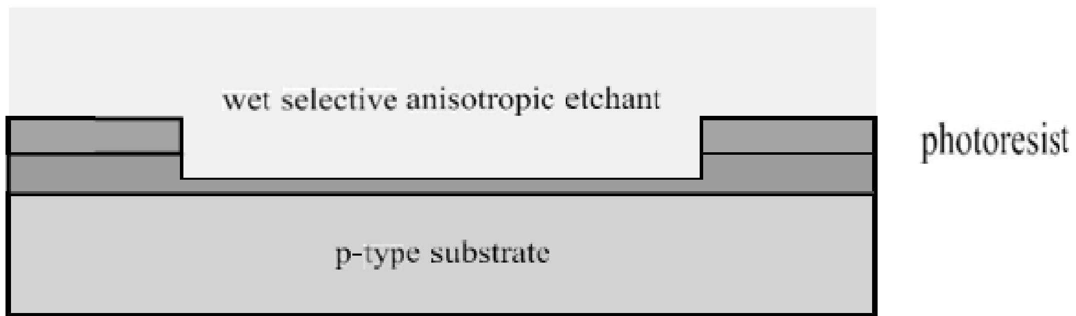
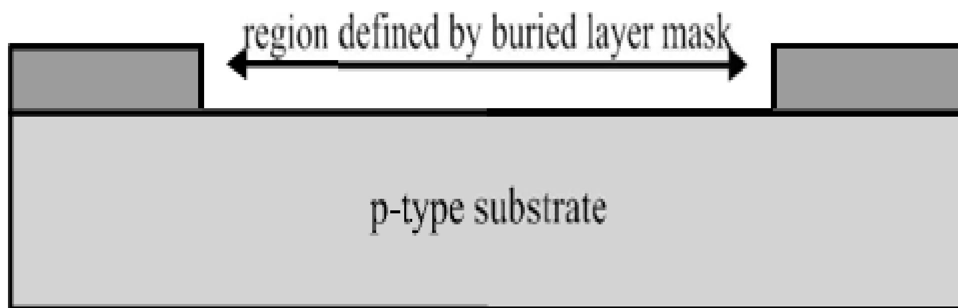
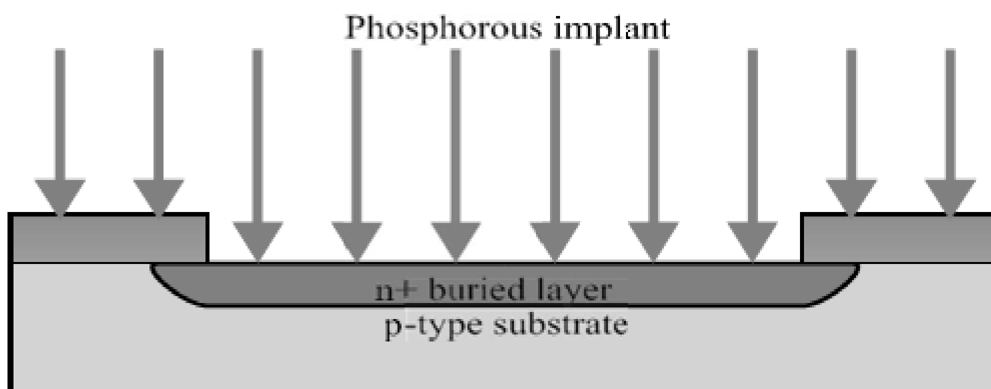


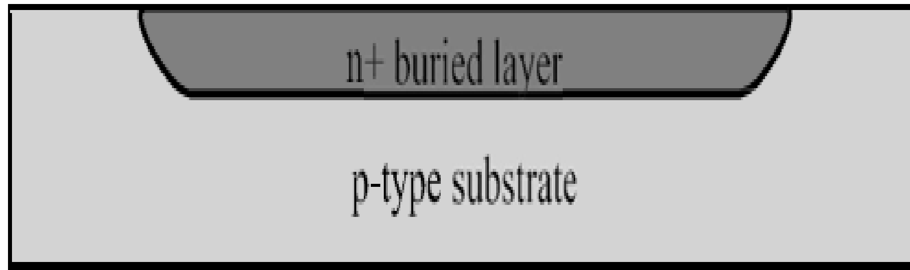
5. **The final buried layer window:** After the left over photoresist is stripped, the deposited oxide has an opening etched within the location provided by the buried layer mask.



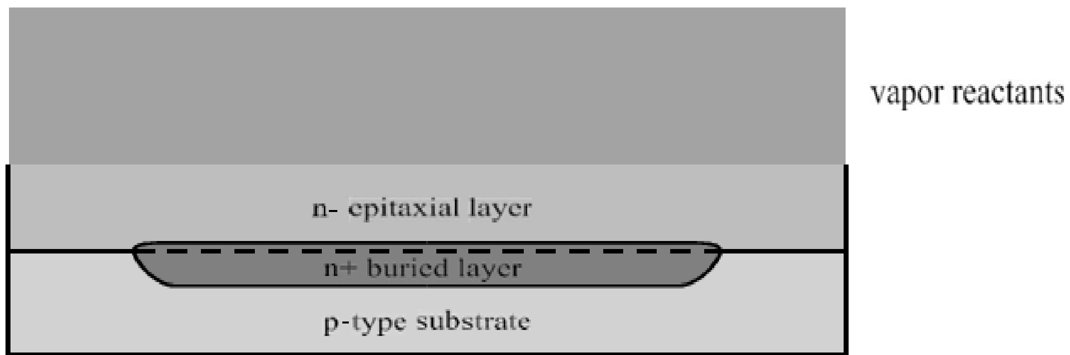
6. **Implant of buried layer:** The buried layer is fashioned with a excessive density (dose) implant of n-type dopant, typically phosphorous. A few lateral diffusion of dopants takes area in the course of the implant. Dopant is also brought into the overlaying oxide.



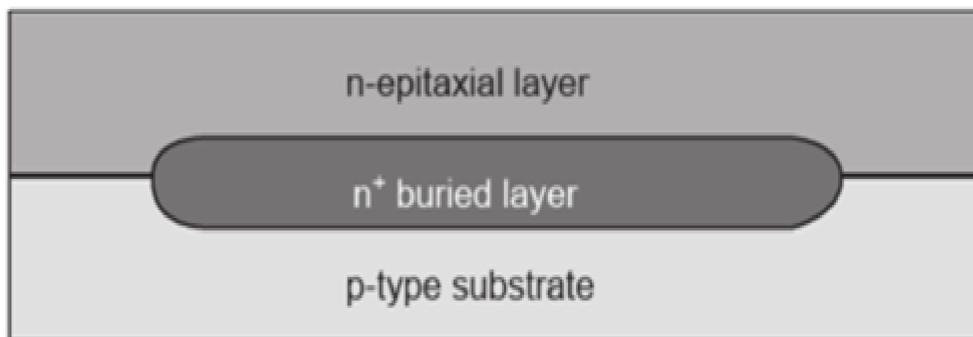
7. **The final buried layer:** After the overlaying oxide is eliminated (etched), the result is a surprisingly doped buried layer place in the unique silicon substrate.



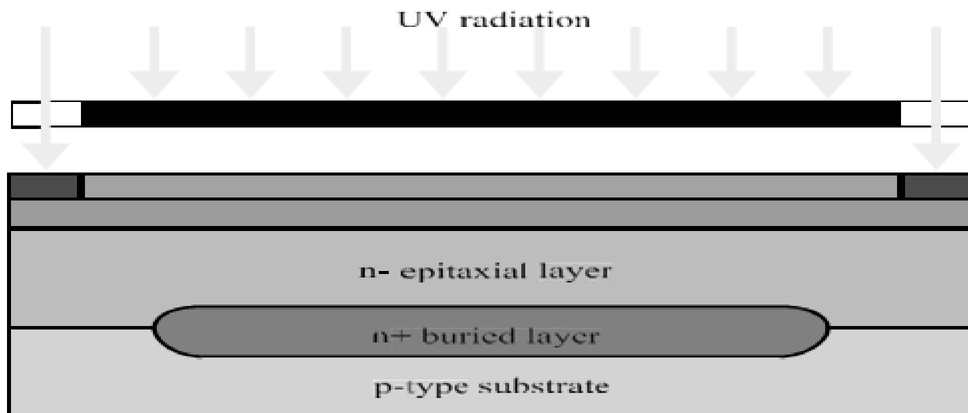
8. **Deposition of epitaxial layer:** Using epitaxial deposition (just like CVD), a layer of very excessive high-quality (crystalline) silicon is deposited at the surface. Some diffusion of dopants happens from the tremendously doped buried layer into the greater lightly doped epitaxial layer.



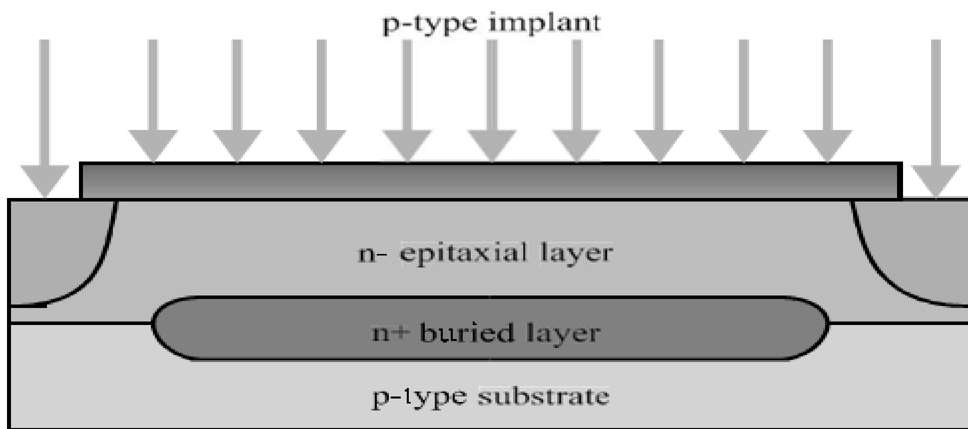
9. **The final Epitaxial Layer:** The resulting epitaxial layer will shape the collector location within the BJT, with the highly doped buried layer forming an equipotential region under the device. The buried layer is now completely enclosed in silicon fabric. 4



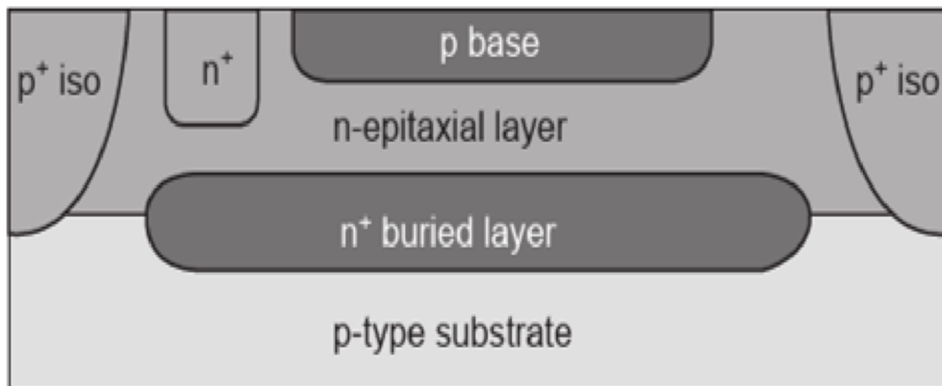
10. **Isolation of the exposure region:** Layers of masking oxide layer and photoresist are fashioned at the surface. The photoresist is uncovered or exposed using an isolation implant mask.



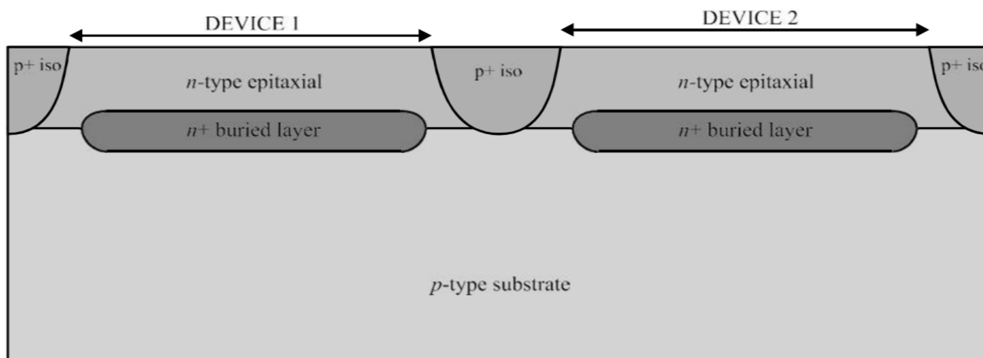
11. **Isolation implantation:** A heavy p-type doping through ion implantation forms the p+ isolation regions. Implantation between the isolation regions is prevent by masking oxide which absorbs dopant.



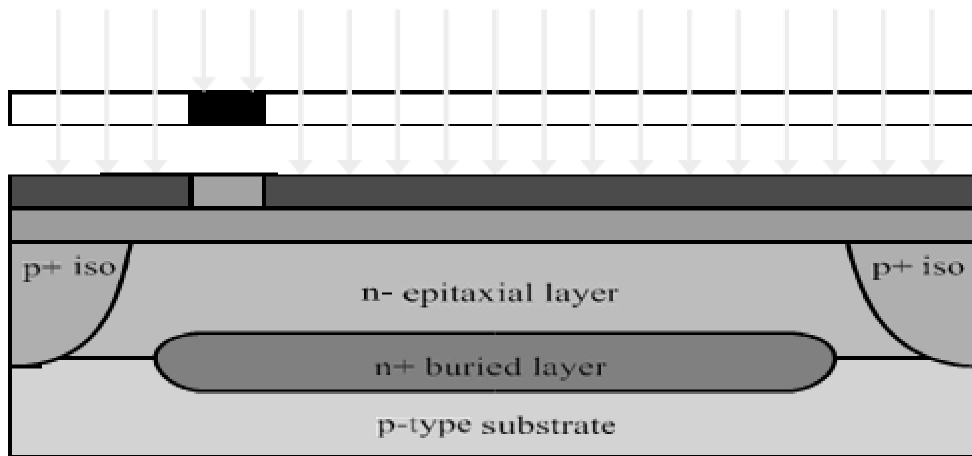
12. **Final isolated structure:** Once the isolation reaches the underlying substrate the masking oxide is removed.



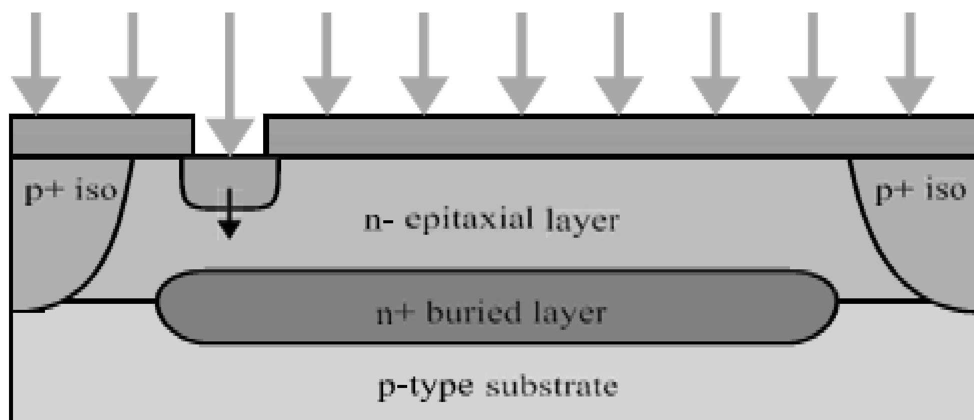
13. **Illustration of p$^+$ isolation:** Through connecting to the underlying substrate, the p+ isolation implants electrically disconnect regions of the epi layer from every other. The pn junction formed between the p+ implants and the n type epi layer provides the isolation electrically.



14. **Sinker mask exposure:** Connection may be made to the buried layer (collector) by usage of a sinker, an implantation of high concentration and significant depth. Oxide and PR layers are exposed through a sinker mask.



15. **Sinker implantation:** N type impurities are implanted into the window etched in the oxide to form a sinker.



16. **Final sinker structure:** Whether the sinker will reach down the buried layer or not depends on the condition of the implantation and thickness of the buried layer.

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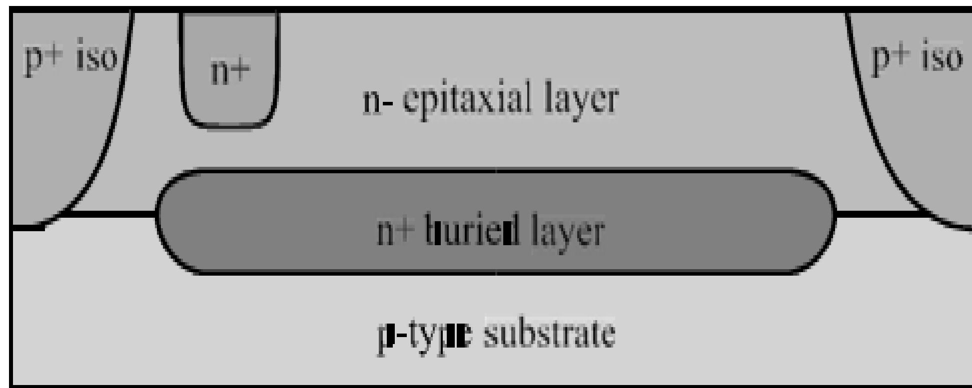
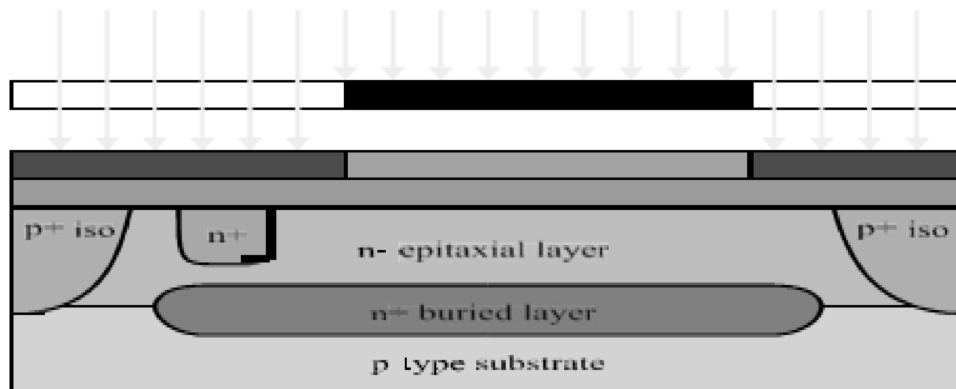
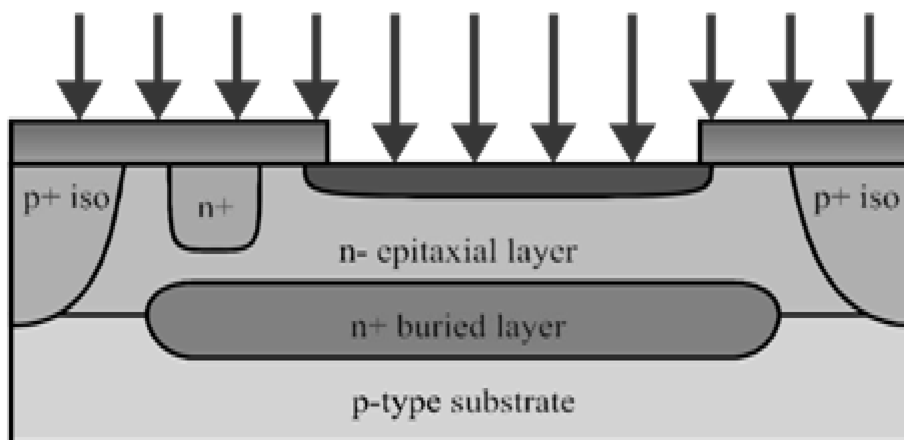


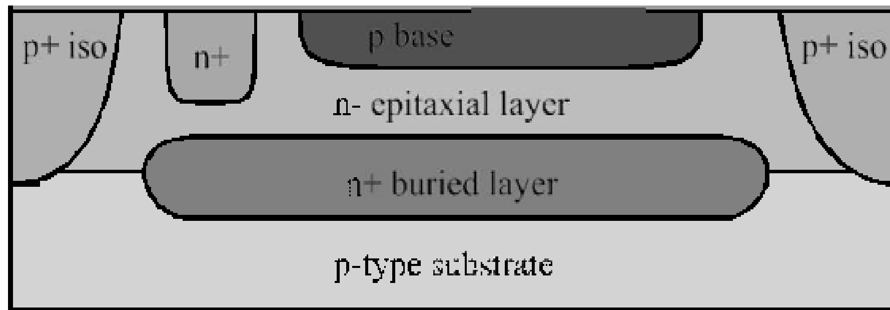
17. **Base mask publicity:** The oxide is formed and the region in which active base has to be formed is exposed using the base mask.



18. **Base area implantation:** Implantation is performed into the epi layer using a p type impurity (usually boron) through the oxide window and p type base region is formed.

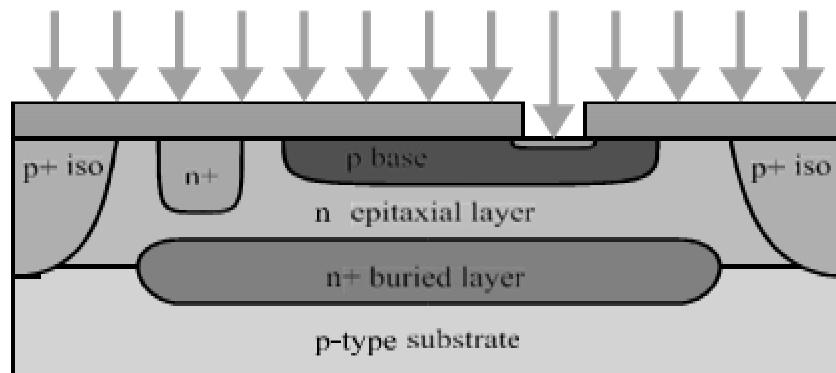


19. **Final base region:** After base area implantation is complete, a counter doped base region has been created in the n-type collector.

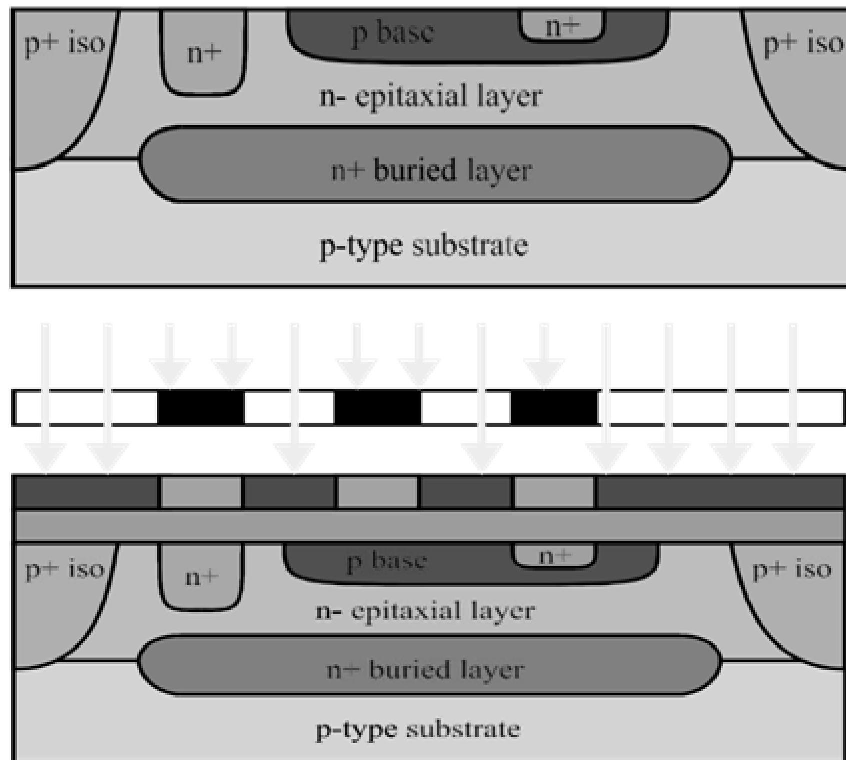


Now the Emitter Region Exposure PR layers are exposed using an emitter mask on the glass plate.

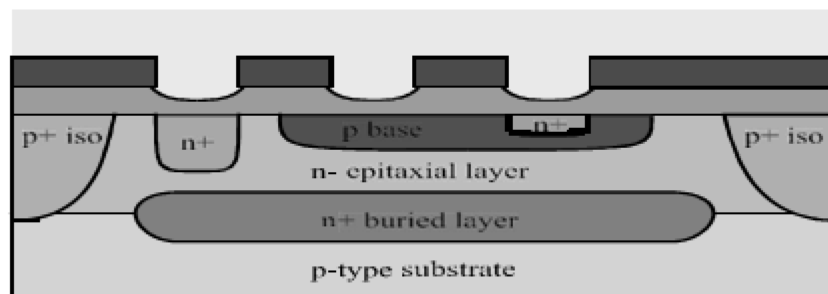
20. **Emitter implantation:** A very heavy n-type dopant (usually Arsenic) is implanted through the oxide opening to form the emitter. It is quite critical for the BJT's working.



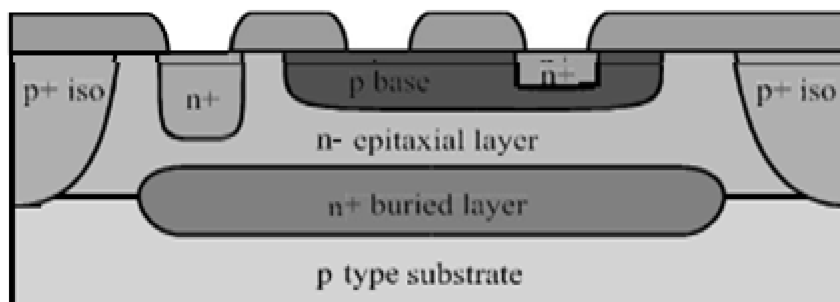
21. **At the end emitter structure and contact cut exposure:** N^+ emitter region in the p-base completes the basic BJT structure, only metal contacts remain. Now thin Oxide is deposited which will isolate metal connections. Photo Resist is exposed using contact cut mask.



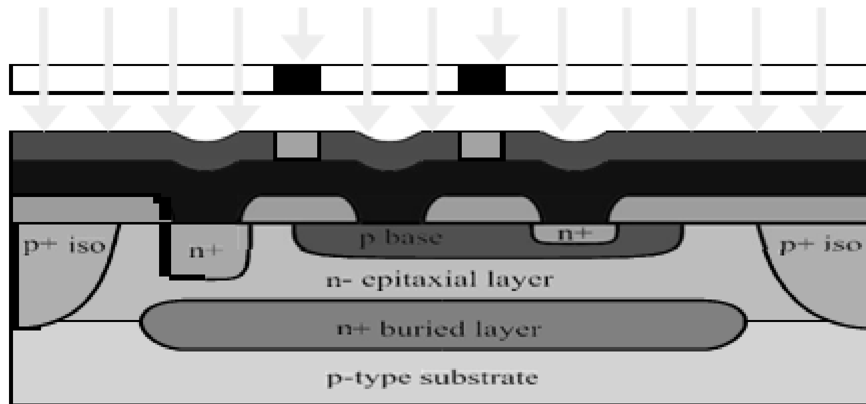
22. **Contact etching:** This openings requires selectivity so etching process does not remove emitter region, therefore wet Chemicals used.



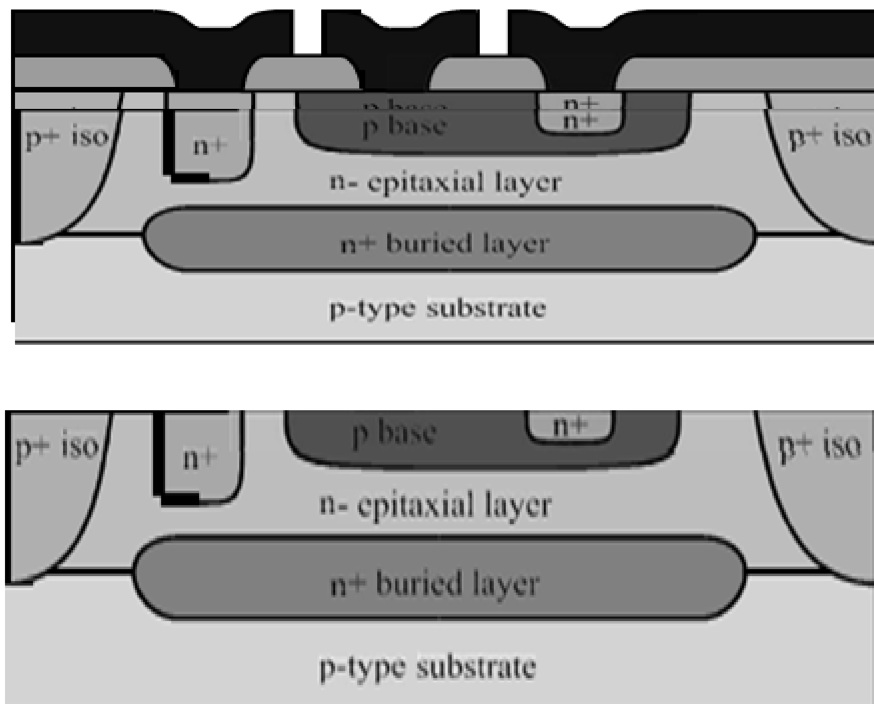
23. **Final contact cuts after etching:** Openings have been created in the oxide layer which will allow access to the collector, base and emitter regions.



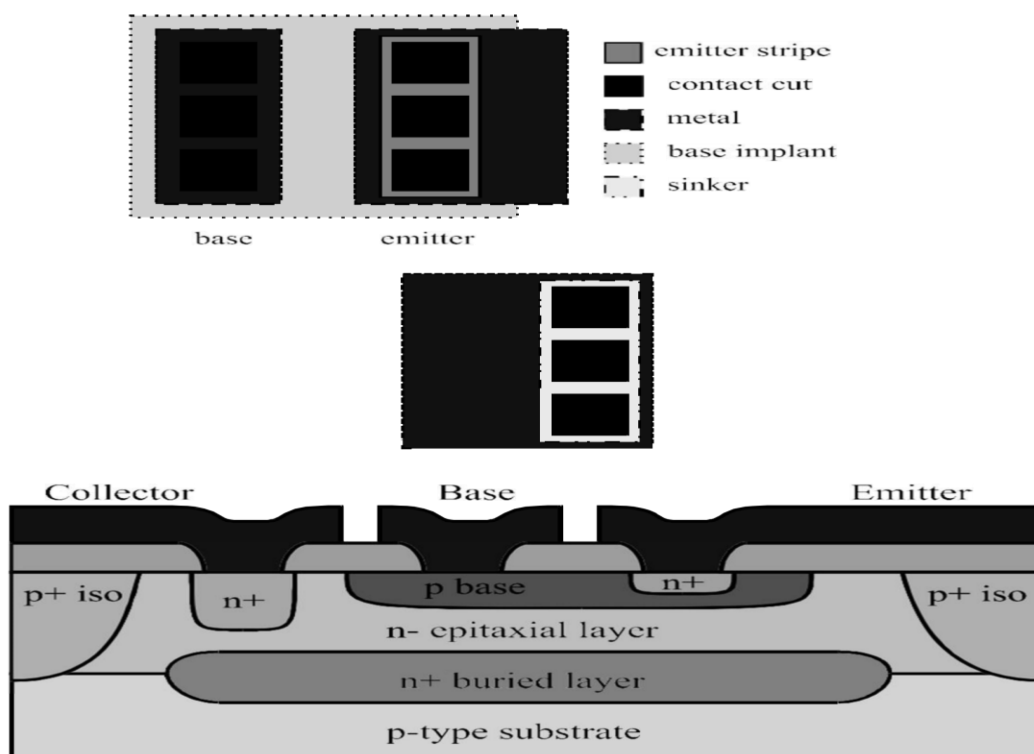
24. **Metal deposition and its exposure**: After metal is deposited and Photo Resist formed on the surface, the exposure is performed with the help of a metal mask.



25. **Final interconnect structure:** As the metal has been etched to form the interconnections between contacts, the final structure is complete. The Modern processes would use more than one layers of metal.



26. **Single emitter, base and collector regions:** Top view shows the various masks used to realize the structure. The Cross section is duplicated to show the correspondence. Buried layer and the isolation masks can be generated automatically by based on size of base region and position of collector region.



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