ASYMMETRICAL MULTI-LEVEL DC-LINK INVERTER FOR PV ENERGY SYSTEM

Abstract

The global shift towards renewable energy sources necessitates innovative solutions to enhance the performance and efficiency of photovoltaic (PV) energy systems. This chapter presents a novel Asymmetrical Multi-Level DC-Link Inverter designed to address the challenges associated with traditional inverters in PV applications. The proposed inverter ,architecture leverages an asymmetrical multi-level topology to improve power quality, reduce harmonic distortion, and enhance overall system reliability. The asymmetrical multi-level DC-link inverter integrates advanced control algorithms to optimize energy conversion and grid interaction. By utilizing multiple voltage levels in the DC-link, the inverter achieves finer voltage resolution, resulting in improved waveform quality and reduced switching losses. This innovation contributes to increased energy yield and a more stable integration of PV-generated power into the grid.

This chapter explains the theoretical foundation and design methodology of the proposed asymmetrical multi-level DC-link inverter. Simulation results demonstrate the effectiveness of the inverter in real-world PV energy applications, confirming its potential to significantly enhance the mperformance, efficiency, and grid compatibility of solar power systems in the pursuit of a sustainable energy future.

Keywords: Photovoltaic, harmonic distortion, solar power, renewable energy.

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I. INTRODUCTION

This chapter introduces a photovoltaic (PV) energy system with two modified maximum power point tracking (MPPT) algorithms by eliminating the proportional and integral (PI) controller, a reduced switch 15-level inverter and a capacitor balancing/ capacitor compensation circuit (CC).

II. BLOCK DIAGRAM OF ASYMMETRICAL MULTI-LEVEL DC-LINK INVERTER

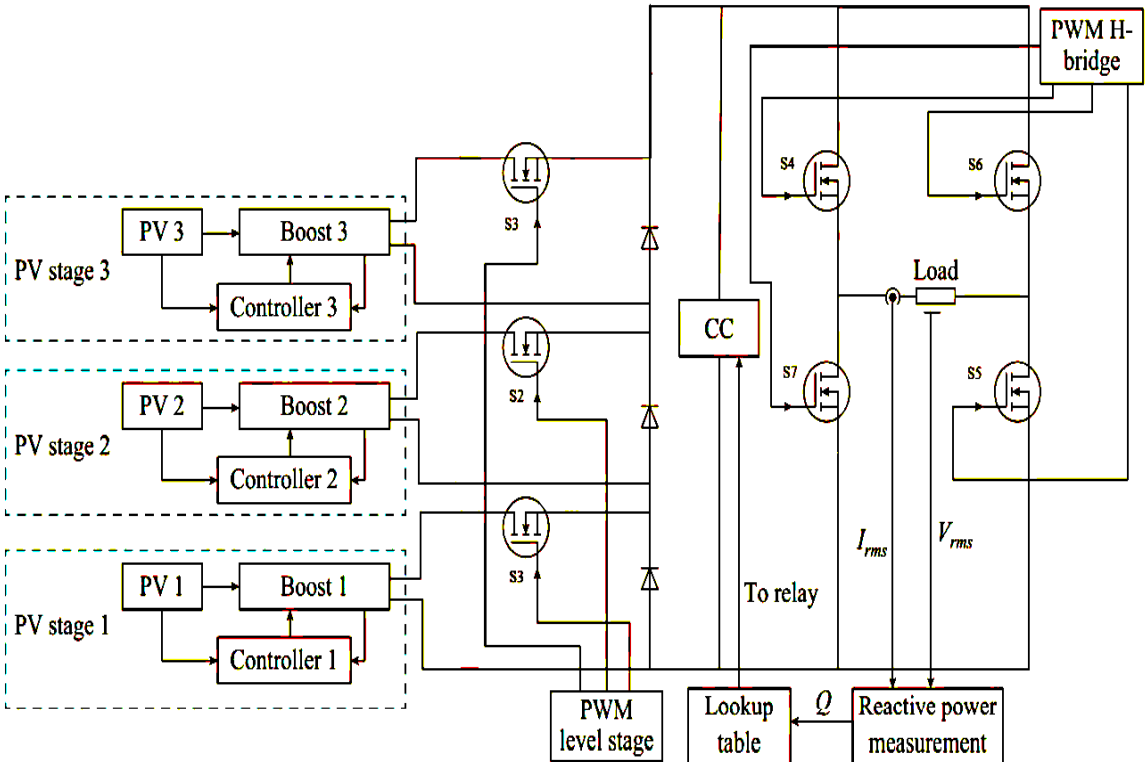

Figure 1: Block Diagram of the Topology

The Asymmetrical Multi-Level DC-Link Inverter topology as shown in Fig.1, it can be divided into three major stages [1-2], they are PV stage: it is responsible for the generation of constant DC supply to the inverter, inverting stage: it responsible for converting DC to AC supply and it is supplying to the load and the capacitor compensation (CC) circuit: it is responsible for providing capacitor balancing in case of reactive loads. The Asymmetrical Multi-Level DC-Link Inverter is broadly classified as

- PV Module
- MPPT Controller
- Boost Converter
- 15-Level Asymmetrical DC-Link Inverter
- Capacitor Compensation

1. **PV Module:** In this section the detailed design parameters of three 100.125 Wp PV Arrays are used to supply the asymmetrical inverter. Each array supplying the specific voltage level the parameters are shown in Table 1.

Table 1: Parameters of PV Panel Model

Parameter	Value
Maximum Power P_{mpp} (Wp)	100.125
Voltage at MPP V_{mp} (V)	18.75
Current at MPP I_{mp} (A)	5.34
Open Circuit Voltage V_{oc} (V)	22.53
Short Circuit Current I_{sc} (A)	5.7
Temperature Coefficient of V_{oc} (%/oC)	-0.35
Temperature Coefficient of I_{sc} (%/^{o}C)	0.05
Temperature of Normal Operation cell (^{o}C)	25

2. **MPPT Controllers:** Two modified MPPT algorithms are explained in this section with their modified flow charts. The usage of a PI or FUZZY controller is no longer required with this improved technique. These algorithms do voltage regulation on its own, making it a stand-alone control system for regulating the voltage of a PV array without the need for a separate controller. Two MPPTs, Perturb and Observe and Incremental Conductance are used and explained in this chapter [3-5].

The modified algorithms for the aforementioned MPPTs are:

- **Perturb and Observe (P&O) MPPT:** The modified flow chart of P&O is shown in below Fig. 2. The main difference between the normal and modified algorithm is the inclusion of a voltage inspection stage. The voltage inspection stage is added after the comparison of power, in the two possibilities. After the inspection stage the voltages are compared and then the increment or decrement of duty cycle is decided [4-7].

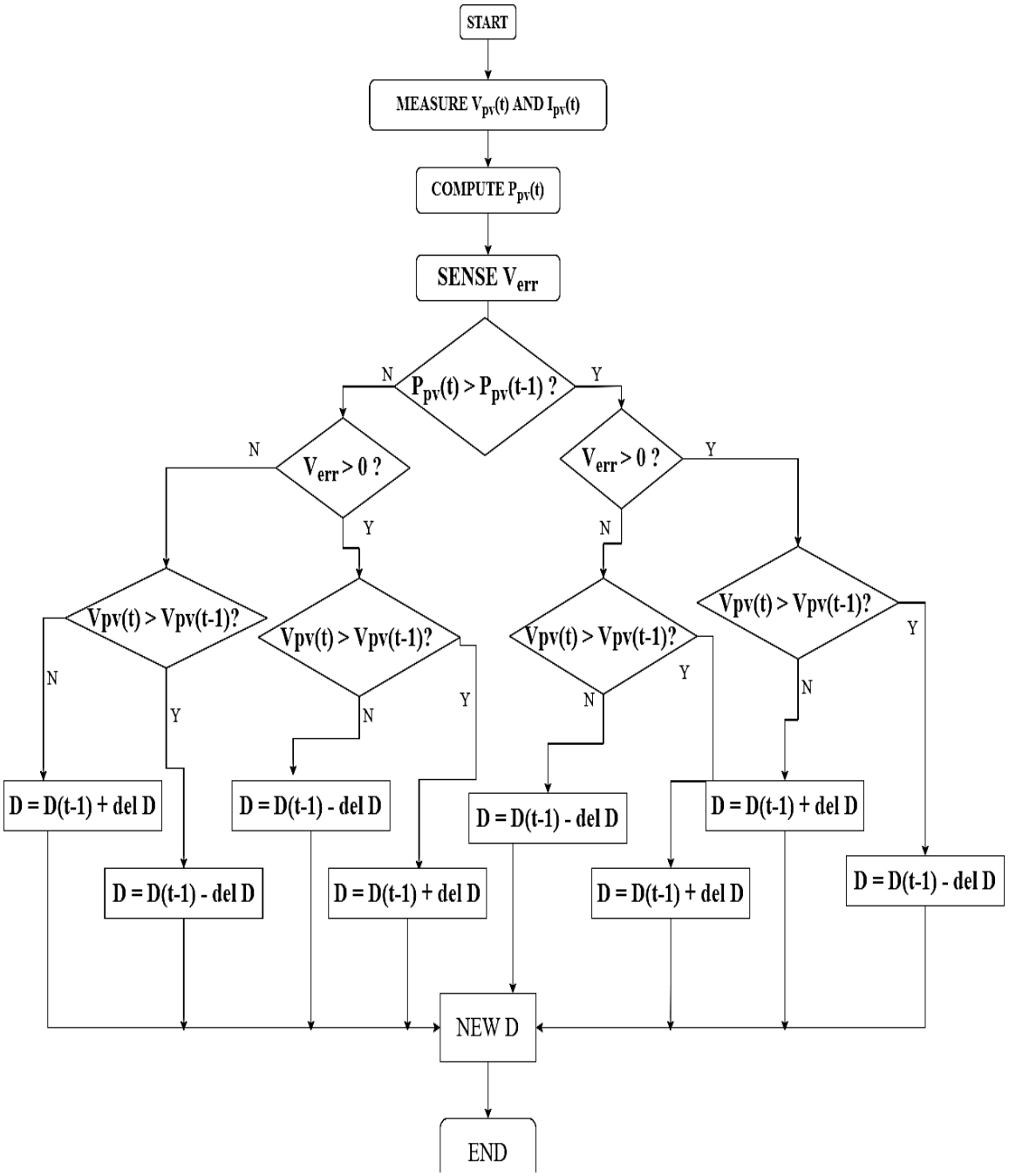

Figure 2: Modified Perturb and Observe MPPT Flow Chart

- **Incremental Conductance (IC) MPPT:** The modified incremental conductance flow chart is shown in the below Fig.3. The modified algorithm of the Incremental Conductance MPPT is given, unlike Perturb and Observe and Hill Climbing MPPT it does not include a power comparison stage. A single voltage inspection stage is added before the voltage comparison stage. After the inspection stage the voltages are compared, based on the possibilities, the increment or decrement of duty cycle is decided [4-8].

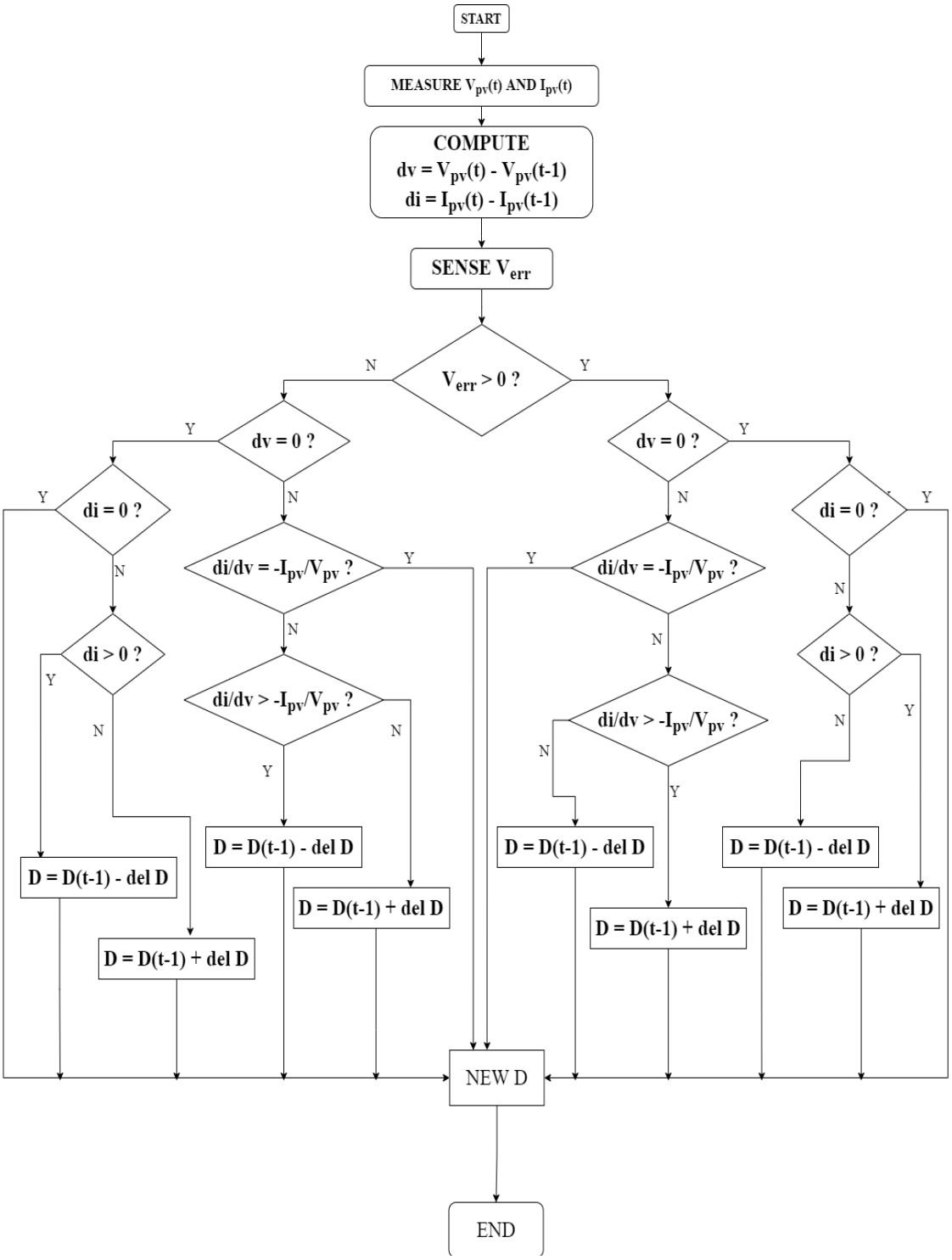

Figure 3: Modified Incremental Conductance MPPT Flow Chart

3. **Boost Converter:** A boost converter is used as a DC-link to the inverter. This boost converter is controlled by the modified MPPT based controller. This controller modifies the duty cycle of the semi-conductor switch of the boost converter in order to control the output DC voltage, which serves as the input to the 15-level asymmetrical DC-link inverter. This is to produce a constant and stable DC voltage to the inverter.

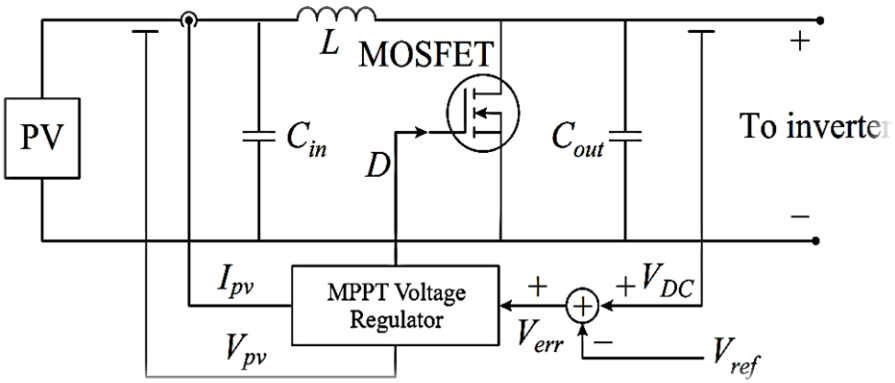

Figure 4: DC-DC Boost Chopper with MPPT Controller

4. **Multi-Level Asymmetrical DC-Link Inverter:** A reduced switch multi-level inverter is discussed. This inverter uses (N-1)/2 switches and different voltage sources, forming an asymmetrical configuration, to generate a multi-level output AC voltage.

The different voltage sources are supplied from the MPPT controlled boost converter, which acts as the DC-link to this inverter. By changing the number of switches at the level stage of the inverter the number of levels can be changed, four switches give 31-level output and by removing one switch the inverter operates in 15-level. As shown in Figure 5.

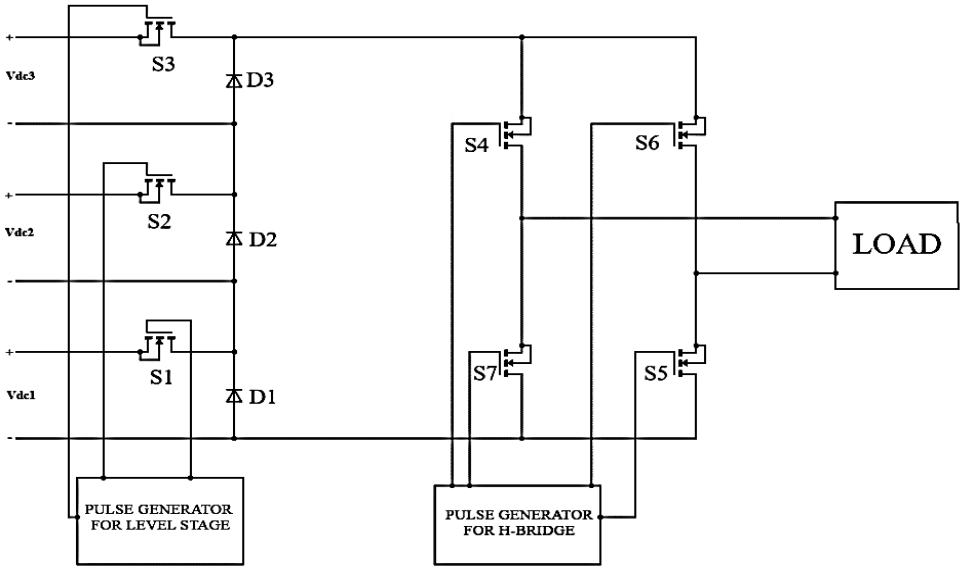

Figure 5: 15-Level Asymmetrical Inverter

In this inverter, switches S1, S2 & S3 acts as the level deciding stage. These switches are responsible for generating the level voltages. These switches are fired according to the voltage required up to the 15-levels, whereas, the switches S4, S5, S6 & S7 acts as an H-bridge and decides polarity of the output AC voltage. Below are the switching sequences of the inverter.

Table 2: Switching States for 15-Level Inverter

	S1	S2	S3	S4	S5	S6	S7
7Vdc	1	1	1	1	1	0	0
6Vdc	0	1	1	1	1	0	0
5Vdc	1	0	1	1	1	0	0
4Vdc	0	0	1	1	1	0	0
3Vdc	1	1	0	1	1	0	0
2Vdc	0	1	0	1	1	0	0
1Vdc	1	0	0	1	1	0	0
0	0	0	0	1	1	0	0

Here, the input DC voltages are taken in binary configuration, 1Vdc, 2Vdc & 4Vdc. The combination of these three voltages gives the levels from 1Vdc to 7Vdc. The switches S1, S2 & S3 are operated in binary sequence to generate the levels. The switches S4, S5, S6 & S7 are operated in such a way that for positive half cycle only switches S4 & S5 are turned ON and for negative half cycle switches S6 & S7 are turned ON.

5. **Capacitor Compensation:** The output current of an inverter lags the output voltage by an angle alpha at an inductive load. The output power is negative in the interval between zeros and alpha. For the application of switch-diode based MLDCL topology, this phenomenon creates voltage spikes in the output voltage waveform. A CC circuit is installed between the first and second stages of the inverter to address this problem. It works by delivering leading power factor components to compensate for the inductive loads' lagging power factor components.

CC circuit is made up of six capacitors that are connected in series by relays. To avoid adding extra power switches to the existing topology, relays are utilised instead of switches, and the system is ideal for low-voltage applications. The following equation can be used to determine the value of compensating capacitors C,

$$C = \frac{Q_C}{2\pi f V^2}$$

1 µF, 2 µF, 4 µF, 8 µF, 16 µF, and 32 µF are the capacitor values used in this section. Capacitance values ranging from 1 to 63 µf are possible with this combination, the CC circuit as shown in Fig.6. The designed CC circuit can generate compensating reactive power in the range of 0.0167 kVAr to 1.047kVAr.

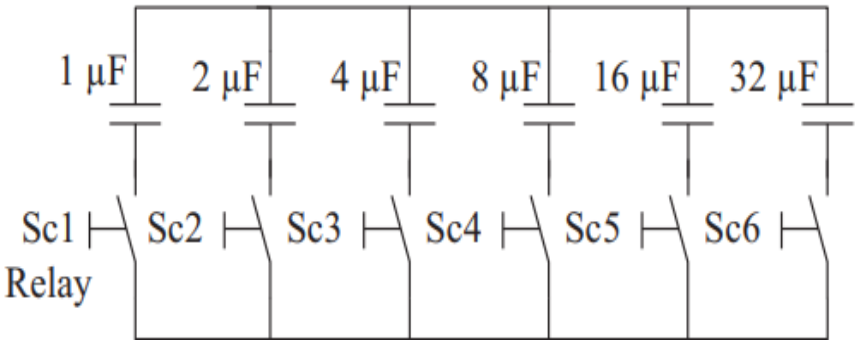

Figure 6: Capacitor Compensation Circuit

The operation of CC circuit can be divided into four modes they are:

- **Mode 1:** In this mode of operation due to load inductance the bus current I_{bus} flows from the load to the CC circuit via the freewheeling diode of S4 and returns to the load via the freewheeling diode of S5. Because I_{bus} is blocked by the diodes and cannot be returned to the sources, I_{CC} serves as the return current, as shown in Fig.7 (a).
- **Mode 2:** In this mode switch S4 carries I_{bus} to the load, while switch S5 carries it back to the source. I_{CC} flows in the same direction as the CC circuit, from CC to S4, and then back to S5, as shown in Fig.7 (b).
- **Mode 3:** Due to inductive load, I_{bus} flows from the load to the CC circuit via the freewheeling diode of S6 and returns to the load via the freewheeling diode of S7. Because I_{bus} is blocked by the diodes and cannot be returned to the sources, I_{CC} serves as the return current, as shown in Fig.7 (c).

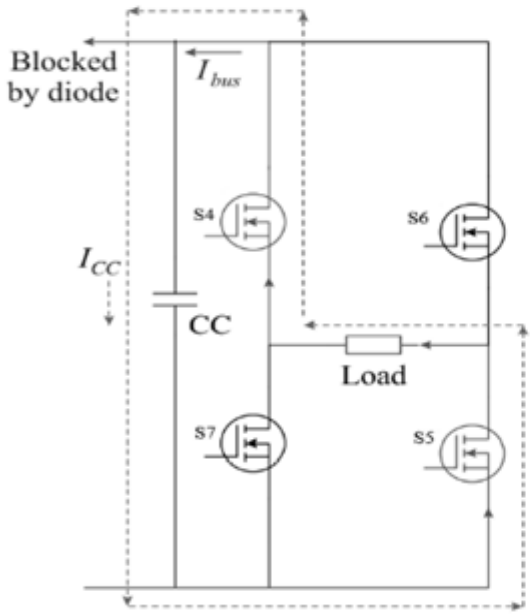

Figure 7 (a): Mode 1 Operation

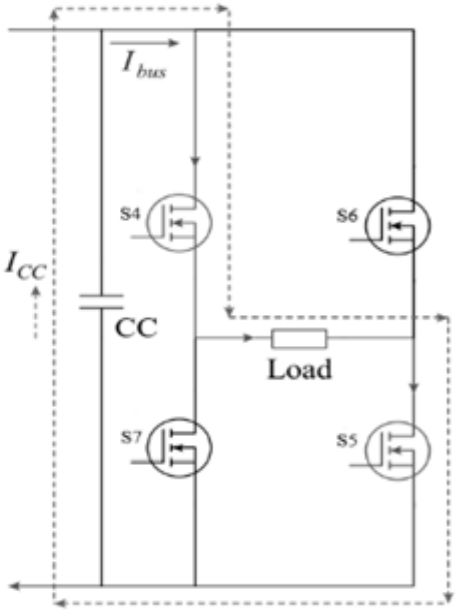

Figure 7 (b): Mode 2 Operation

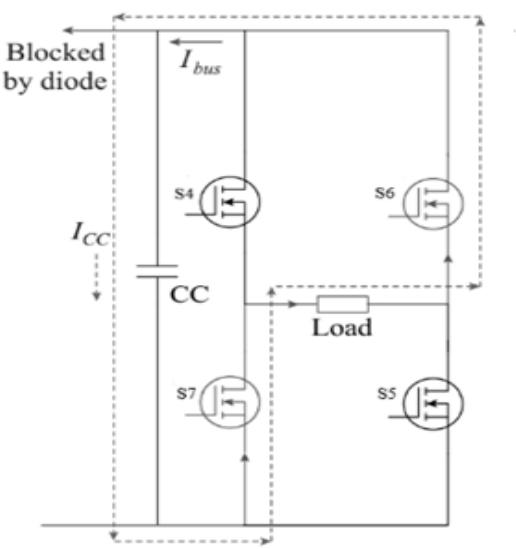

Figure 7 (c): Mode 3 Operation

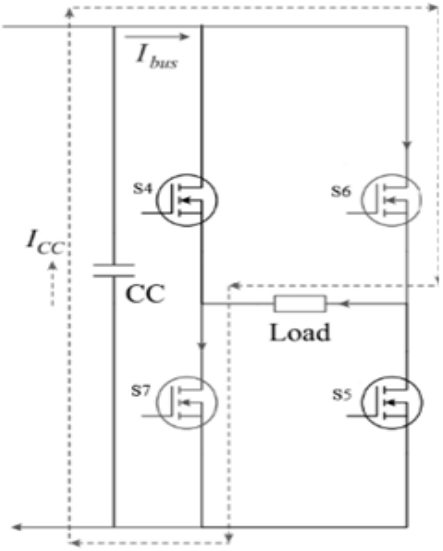

Figure 7 (d): Mode 4 Operation

- **Mode 4:** In this mode the switch S6 carries I_{bus} to the load, and S7 carries it back to the source. I_{CC} travels in the same way as the CC circuit, from the CC circuit to S6, and then back to the CC circuit through S7, as shown in Figure 7 (d).

III. CONCLUSION

In this chapter it concludes that, the detailed calculation, values and analysis of PV array, modified flow chart of Perturb and Observe (P&O) & Incremental Conductance (IC) and 15-levels Asymmetrical DC-link voltage control and the reactive power compensation of the load with Capacitor Compensation (CC) circuits were analyzed.

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