Laxmi Kolakar
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PROFESSIONAL SUMMARY:

➢ 10+ years of experience as Post Silicon Validation ATE Test Lead. Experienced in working on testers: Advantest 93K, Teradyne [Uflex, Iflex and J750]. Worked with the team for test programs bring up and release to production.

Company: TESSOLVE Semiconductors Pvt Ltd, Bangalore. [Period: April 2011 – till date]

Skills

- ➢ Hands on experience in Advantest 93K, Teradyne [Uflex, Iflex and J750]
- ➢ Feasibility check for ATE testing, SOW preparation & weekly schedule update to customer.
- ➢ Schematic review and Layout review using Allegro software
- ➢Test program development for FT, WS and CHAR blocks.
- ➢ Converting from Single site to Multi site solution thereby increasing Production Capacity.
- ➢ Device characterization like PVT, Shmoo data collection & data analysis.
- ➢ Simvision tool knowledge to view the signals for vcd , wgl file
- ➢ Data analysis tool knowledge: SEDANA and In-house tool.
- ➢ Good knowledge on revision control tools: SVN and GIT.
- ➢ Proficient to solve the run time program issues and
- ➢ Lead the junior's team to train & work on the 93k tester platform and Teradyne platform.
- ➢ Training freshers for the ATE basics and Testing fundamentals.

Roles & Responsibilities

➢ **Test Lead. Test Engineer, Sept 2018 – till now**

Ethernet Port - (ADI Onsite support)

- Pattern Conversion [Running Simulation, creating vcd file and VCD to atp file generation].
- Developed test program for SPI functional and char tests like setup, hold and delay time measurement.
- Conversion from single site to multi-site program
- Test time reduction activities [64sec to 16 sec] by converting VBT test method to pattern based testing

PMIC (portable home entertainment equipment) – (Dialog Semiconductor)

- Developed the test programs (C++) for various pmic blocks such as BUCK, LDO, SWITCH and program bring-up Includes various Trim (voltage/current/frequency), DC Measurements & Fusing.
- Analysis of test results with designers and provide High-quality test, bug reports and debugged the test programs in splits corners & temperature.
- Optimize and automate test programs by applying more efficient testing methods to reduce product test times and manufacturing cost. Worked on GRR, Yield enhancement, report presentation and program release to the factory Cooperate with product/equipment engineering teams to improve overall product yield and customize available test solutions.

Mobile Chip:

• Worked on Memory failure analysis, Different lot wafer data collection, failing bit identification using with algorithm.

➢ Sr. Test Engineer, April2014 – Aug2018

WLAN Devices [Broadcom India Onsite support for 1year]

• Handled different device version program SVN restructure and wafer screening using Prober remotely and yield monitoring and improvement.

Router chip [93K Platform]

• Worked on CPR block [Core power reduction] functional bring up and characterization across voltages and CPR values fusing support

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➢ Test Engineer, April 2011 – April 2014

Modem chip [93K Platform]

- Developed the test program for structural [Jtag and BSDL] and functional vectors.
- Closely working with Design team to bring-up the structural and AVS [adoptive voltage scaling] char test, analyzed & present the shmoo, vmin/fmax margin report to design team.

APU/GPU [93K Platform] [AMD Singapore Onsite for 1 year]

- Program bring up, validation and release for offshore.
- bring up of functional core and supported Advantest team to bring up DAC code, yield analysis and TTR debug.

8 Bit Single Chip Microcontroller [J750 Platform]

- Conversion project from 4 site solution to 16 site solution. Challenges faced using 1024 channel board dock on 512 channel tester, Achieved high parallelism with reduced test time

ACADEMIC DETAILS

➢ B.E (ECE) with aggregate of 78 % from VTU university SDM CET Dharwad College.

RECOGNITIONS

- Awarded for the Excellent support on Digital phasing for the SOC project.
- Appreciated for the Excellent support on Broadcom 4349 Project.
- Awarded the most competent worker for test time reduction on Wi-Fi chip from 40 seconds to 19 seconds in production program
- Collaboration across teams for forecast and scheduling to deliver on time.