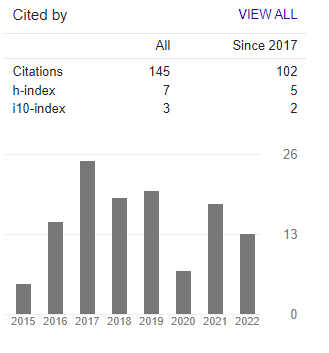
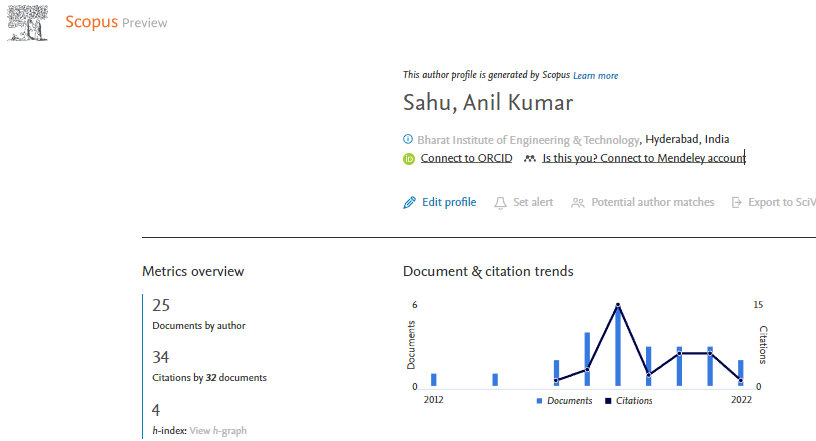
** **

**Curriculum Vitae**

1. NAME : **Dr. ANIL KUMAR SAHU**

2. Father’s Name: SHRI. NAROTTAM LAL SAHU

3. . Date of Birth : 12-08-1982

5. Present Postal Address : Prof. (Dr.) A. K. Sahu

HIG-I/43, Nirmala Kunj Old Borsi , Durg (Chhattisgarh)

Ph: 91- 9926811371(M), 7987740974(Jio-M)

**Email: anilsahu82@gmail.com,**

6. Nationality: Indian

7. Educational Qualifications**:** **BE Electronics and Telecommunication Engineering , M. Tech. Microelectronics and VLSI design (Honors), Ph.D(Awarded) in Electronics and Telecommunication ,PG Diploma in AI and ML (NIT Warangal)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Degree** | **Subject** | **Board/University** | **Year** | **%** | **Division** |
| **Post Graduate Diploma** | Artificial Intellegent (AI )and Machine Learning(ML) | National Institute of Technology Waranagal,Telangana  (Association with  Edureka) | **2023** | **3.71/4 credit** | |
| **Ph.D.** | Electronics and Telecommunication Engineering | C.S.V.T.U ,Bhilai(C.G) | **15 DEC 2018** | **PhD Awarded** | |
| **M. Tech.** | Microelectronics andVLSIDesign | Shri G.S. Institute of Technology and Science.R.G.P.V. Bhopal(M.P) | 2008 | 77.27 | 1st Division (Hons.) |
| **B.E.** | Electronics and Telecommunication | C.S.I.T Durg/Pt. R.S.S .U.Raipur (C.G) | 2005 | **73.93** | 1st Division |
| **Higher Secondary** | P. C. M. | Board of Secondary Education, Bhopal | 2000 | 70 | 1st Class First in M.P. Board Exam, Bhopal *(Topper in patan Town)* |
| **High School Examination** | Hindi, English, Mathematics, Science, Social Science, Sanskrit | Board of Secondary Education, Madhya Pradesh, Bhopal | 1998 | 75 | 1st Class (Hons) |

**Annexure-1**

**Total Teaching Experience: 15 year 5 months**

1. Lecturer in ETC (from 10-5-2005 to 1-7-2006 , total 1Year 2 months) at **D.N. PATEL ENGG. COLLEGE NANDURBAR, Shada, (M.H)**.
2. Lecturer in ETC (from 1-7-2008 to 31-5-2009, total 6months} **in CIIT (RKDF groups) Engg. College indore (M.P.) .**
3. **Assistant Professor in Asst. Professor at SSTC- Shri Shankaracharya Groups of Institution Bhiali,(Chhattisgarh),India** from 22-6-2009 to **27-11-2019**, Total 10 year 05 month) .
4. Associate professor (from 17-12-2019 to  **12-05-2023.**, Total 3 Year 6 month) at **Bharat Institute of Engineering and Technology Hyderabad ,Telanagana ,India.501510**

**M. Tech Dissertation**

**“**BIST Controller Architecture for testing and Diagnosing Interconnect

Fault in FPGAs **”**

**Coding style** - Verilog 1995.

**Synthesis Tool** - Precision Synthesis in FPGA advantage HDL Designers.

**Simulation Tool** - Modelsim III XE version 6.1c.

**Verification Tool** - Mentor Graphics and Vera of Synopsys.

**Description:**

Built in Self-Test Controller model includes faults analysis & scan insertion application, which embeds much of the tester functionality in to the device itself. A BIST Controller is inserted into the design essentially applies a series of Scan Pattern to be generated by self enabling test patterns generator & then response are captured by response analyzer.

This thesis also presents the comparison of Controller design in ASIC/FPGAs. We also investigate the impact of different BIST Controller architecture while keeping in to the mind of testing the design with internal mechanisms.

**Ph.D Dissertation**

“System Level Behaviral modeling and Post Simulation of Built in self test of sigma delta modulator ADC”.

Many Evaluation of M.E./M.Tech Dissertation Work is being done

**M.Tech Candidates Working Under Anil Kumar Sahu: Total = 30**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **S.N.** | **Student Research - Masters Degrees** | | | | | | |
|  | **Name of Student** | **Year of Completion** | **Title of Thesis** | **Co-Investigators (if any)** | | |  |
| 1. | **Amrita Kumari** | 2012 | Desiging and Implementation of Linear Feedback shift register and Its Analysis | NIL | | |  |
| 2. | **Garima Pandey** | 2016 | Resetting 2-Order Sigma –Delta Modulator in130 nm CMOS Technology | NIL | | |  |
| 3. | **Bhavesh Sahu** | 2016 | FPGA Implementation of IP-core of FFT Block for DSP Applications | NIL | | |  |
| 4. | **Zeesha Mishra** | 2017 | “A review on architecture of high speed data communication for USB 2.0 device using FPGA” | NIL | | |  |
| 5. | **Reetika Upadhaya** | 2017 | CORDIC enabeled ORA for Sigma delta ADC | NIL | | |  |
| 6. | **Ankita Khurana** | 2016 | Design of Low Power VCO Enabled Quantizer in Continuous Time Sigma Delta ADC for Signal Processing Application | NIL | | |  |
| 7. | **Arpit Tiwari** | 2017 | Low Pass Notch Filter Design for Biopotential Signal Acquisition System” | NIL | | |  |
| 8. | **Y. Tembhre** | 2016 | Testing of an 8-bit Sigma Delta ADC Based on Code Width Technique Using 45nm Technology | NIL | | |  |
| 9. | **R. K. Makkad** | 2016 | Novel design of fast and compact SHA-1 algorithm for security applications, | NIL | | |  |
| 10. | **Vivek Kumar** | 2015 | Design of Single –loop CT Sigma-Delta Modulators for high resolution – wideband applications using GUI" | NIL | | |  |
| 11. | **Prateek Verma** | 2014 | A Graphical User Interface Implementation of Second Order Sigma- Delta Analog to Digital Converter with Improved Performance Parameters | NIL | | |  |
| 12. | **Akansha Sahu** | 2015 | A Review on Multiplier based on Reversible Logic Gate and Vedic Algorithm for Quantum Computing | NIL | | |  |
| 13. | **Jageshwar Prasad Sinha** | 2013 | NEW EFFICIENT REDUDANT RADIX 4 MULTIPLIER DESIGN USING VHDL” I | NIL | | |  |
| 14. | **Chandrashekhar Sahu** | 2017 | linearize VCO-ADC | NIL | | |  |
| 15. | **Rashid Sheikh** | 2018 | Ultra low power design approach of asynchronous delta sigma modulator. | NIL | | |  |
| 16. | **Ashish Tiwari** | 2012 | An innovative approach of computational fault detection using the Desing for Testability of CP-PLL” | NIL | | |  |
| 17. | **Sangita Shit** | 2011 | Design and Analysis of LINAC Control System in FPGA” | NIL | | |  |
| 18. | **Darshana Dongre** | 2011 | Implementation of AXI Design core with DDR3 memory controller for SoC | NIL | | |  |
| 19. | **Arvind Sahu** | 2018 | design of Notch filter for bio sensor application | NIL | | |  |
| 20. | **Swati Singh Solanki** | 2018 | Ultra Low Power Consuming VLSI Architecture for Montgomery Modular Multiplier Using Adiabatic Array Logic | NIL | | |  |
| 21. | **Sapna Soni** | 2018 | Design of Sigma Deta ADC for Biomedical Application | NIL | | |  |
| 22. | **Ankit Jiaswal** | 2018 | DETECTION OF HARDWARE TROJANS FOR MIXED SIGNAL HARDWARE SECURITY | NIL | | |  |
| 23. | **Akansha Pawar** | 2016 | LMS Filter Design | NIL | | |  |
| 24. | **Priyanka Bibay** | 2012 | RTL Design of DDR SDRAM Controller Using Verilog | NIL | | |  |
| 25. | **Rajeev Kumar Singh** | 2015 | Design and Implementation of Discrete Cosine Transform Architecture Blocks | NIL | | |  |
| 26. | **Monika Singh** | 2013 | SNR Reduction of 2nd order Sigma-Delta Modulator Using Genetic Algorithm | NIL | | |  |
| 27. | **Varun sonwani** | 2014 | design of bandpass sigma deta ADC. |  | NIL |  |  |
| 28. | **Venu** | 2021 | VLSI Crpyosystem |  | NIL |  |  |
| 29. | **Cherita** | 2020 | Vedic Multiplier for Signal Processing Unit |  | NIL |  |  |
| 30. | **Monika** | 2021 | MIMO system development |  | NIL |  |  |
|  |  |  |  |  |  |  |  |

#### ACOMPLISMENTS AND AWARD

* Selected in CEERI pilani (Rajasthan) as project assistant for R& D development in Area of Semiconductor & EDS.
* Secured **90** percentile in GATE 2006.
* Best Paper Awrad in Internation Springer Conference ny NIT Mizorem 2022 .
* IBM Hackthoyn Best Runner Up in 2021(Topics: Touch Me Not for Women Safey)

**EDA TOOLS USED**

Xilinx : (Xilinx 8.2i,Xilinx 9.1i, MODELSIM III. 6.1c)

Tanner : (T-Spice, L edit, S edit, W edit).

Synopsys : (CosmosSE, CosmosScope, Signal Integrity,

Prime Time Analysis, design compiler,VCS Simu.)

Mentor Graphics: (FPGA Advantage with Precision Tool,DFT Advisior, Fastscan).

Programming Languages: C, Assembly language, MATLAB 6.5

**computer PROFICIENCY**

Programming Language **:** Python advance and Core ,Java(J-query)

Python for AIand ML,Machine Learning,Predictive Anaysis,DeepLearning,Sequential Learning

Hardware Language : VHDL AND VERILOG(1995).

Scripting languages : Perl, Vera.

Operating Systems: DOS, WINDOWS FAMILY AND LINUX

MarkupLanguage:HTML,CSS,Bootstrap

#### AREAS OF INTEREST

Testing and Verification, Digital Signal Processing (filters) .

VLSI Design –Digital Design, ASIC/ FPGAs Based Design,   
EDA Tools - Physical Design aspect, Layout & Routing related.   
 Communication related algorithms.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **S.N.** | **COURSE TAUGHT:** | | | | | | |
|  | **Name of the Course** | **Level (UG/PG)** | **Year in which taught** | **Class Strength** |  |  |  |
|  | BE | UG | 2009 | 120 |  |  |  |
|  | Mtech(VLSI Design) | PG | 2009 | 18 |  |  |  |
|  | BE | UG | 2010 | 120 |  |  |  |
|  | MTECH | PG | 2010 | 18 |  |  |  |
|  | BE | UG | 2011 | 120 |  |  |  |
|  | MTECH | PG | 2011 | 18 |  |  |  |
|  | BE MICROWAVE COMMUNICATION ENGG | UG | 2012 | 120 |  |  |  |
|  | BE BASIC ELECTRONIS | UG | 2012 | 120 |  |  |  |
|  | BE-LINEAR INTIGRATED CIRCUIT | UG | 2013 | 120 |  |  |  |
|  | BE- DIGITAL ELECTRONICS AND LOGICS | UG | 2013 | 120 |  |  |  |
|  | BE OPTICAL COMMUNICATION AND RADAR ENGG. | UG | 2015 | 120 |  |  |  |
|  | BE- VLSI DESIGN | UG | 2016 | 120 |  |  |  |
|  | BE-MICROWAVE COMMUNICATION AND OPTICAL INSTRUMENTATION | UG | 2017 | 120 |  |  |  |
|  | BE- CONTROL SYSTEM | UG | 2018 | 120 |  |  |  |
|  | MTECH-LOW POWER DESIGN | PG | 2013 | 18 |  |  |  |
|  | MTECH : VLSI SYSTEM DESING AND VLSI SYSTEM TESTING | PG | 2014 | 18 |  |  |  |
|  | MTECH - CMOS CUIRCUIT DESIGN | PG | 2015 | 15 |  |  |  |
|  | MTECH-ALGORITHEM FOR VLSI PHYSICAL DESIGN AND AUTOMATION | PG | 2016 | 18 |  |  |  |
|  | MTECH-MODELLING WITH VHDL | PG | 2017 | 18 |  |  |  |
|  | MTECH-ANALOG CIRCUIT DESIGN | PG | 2018 | 18 |  |  |  |
|  | B.TECH-ICA | UG | 2019 | 90 |  |  |  |
|  | MTECH-LOW POWER VLSI DESIGN | PG | 2019 | 18 |  |  |  |
|  | B.TECH- ANALOG CMOS DESIGN | UG | 2020 | 90 |  |  |  |
|  | MTECH-VLSI SYSTEM DESIGN | PG | 2020 | 18 |  |  |  |
|  | B.TECH- MICRIWAVE AND OPTICAL COMMUNICATION ENGG. | UG | 2021 | 45 |  |  |  |
|  | B.TECH-PYTHON PROGRAMMING | UG | 2021 | 90 |  |  |  |
|  | MTECH-VLSI TESTING | PG | 2021 | 18 |  |  |  |
|  | B.TECH-ARTIFICIAL INTELLIGENT | UG | 2022 | 90 |  |  |  |
|  | B.TECH- MACHIN LEARNING | UG | 2022 | 90 |  |  |  |

**Annexure-2**

**(Administrative/Supervisor Experience)**

1. In charge of Computer Simulation Lab Since June 2010 onward till date .
2. Member of Anti-Ragging Team from 7 years
3. Worked as Hostel visitor from 12th Oct 2010 to till date.
4. Worked as Class In charge of BE 7th and 8th SEM
5. Working as Coordinator ME (VLSI design) of SSGI(FET) ,Bhilai .
6. Worked as Project in charge of ETC Final year.
7. In charge of Departmental Extra Curriculum work such as for Organizing the Conferences
8. Worked as In charge of Training and Placement of ETC .
9. In Charge of ME (VLSI Design) in SSTC.
10. Speaker on one Day Work Shop of “Image processing and VLSI technology “SSTC Bhilai.

11.College level Project Incharge in BIET Hyderabad from 202o Till Date.

12. ECE Deapartment level Project Incharge in BIET Hyderabad from 202o Till Date.

13. Training Incharge for Placements from 2020 to till date.

14.Hakathon Club incharge in BIET from 2022 to Till date.

15.Brand Amessder of IIC Cell In Hyderabad Telangana

16. NBA and NAAC Critera 2 collge level Incharge

17. ARIIA Incharge for BIET Hyderabad

**ANNEXURE-3**

**(RESEARCH EXPERIENCE)**

**PhD Guidance:**

1.**Research Topics**;

“Design and Synthesis of energy aware digital circuit for nanoelectronics and Application ”

**Role** :Co-Supervisor

**Name of Reserch Scholar**: Ravi Tiwari

**University** :State University CSVTU bhilai Chhattisgarh ,India

**Status**:Ongoing

2.**Research Topics**;

“Design and Synthesis of Multi Valued Logic circuit using CNTFET for Low Power Nanoelectronics Application”

**Role** :Co-Supervisor

**Name of Reserch Scholar**: Pradeep Yadav

**University** :State University CSVTU bhilai Chhattisgarh ,India

**Status**:Ongoing

**Annexure-4**

**International Conference/workshop are participated**

**workshop are participated**

1. Attendant workshop in CSVTU Bhilai on title of FPGA Controller Design For Anesthetic Drug delivery system Using Fuzzy system under TEQIP-III programmed.
2. Attend Three Day Online Workshop On Verilog VLSI design by MAVEN SILICON Technology Banglore.
3. Attend Online webinar in Title of Open Access Journal organized by Elsevier Research Academy .
4. Attended One Week FDP (Faculty Training Programmed) in BIT Durg by NITTTR Bopal.
5. Attended One Week FDP (Faculty Training Programmed) in VLSI Design by NITTTR Chandigarh.
6. Attended One Week FDP (Faculty Training Programmed) in Artificail Intteligent by NITTTR Chandigarh.
7. Attended One Week FDP (Faculty Training Programmed) in Reserch methodology by NITTTR Chandigarh.
8. Attended One Week FDP (Faculty Training Programmed) in Claimet Change and Enviornment and by NITTTR Chandigarh.
9. Recevied 22,Coursera Certificate as FDP.
10. Recceived 4 ,IBM course Cerificate as FDP .
11. Attended 25 National webnior and Internation Webnior.
12. Institution Innovation Council(IIC) Member wirh Adavce and Basic Level Certification.

**NPTEL CERTIFICATION:**

1.Awareded Cetification in **Iternet of Things(IOT**) in NPTEL- 12 WEEK Course

2. Awareded Cetification in **Artificial Intelligent** in NPTEL- 12 WEEK Course

3. Awareded Cetification in **Pyhon for Data Analytics** in NPTEL- 12 WEEK Course

4. Awareded Cetification in **ML(Machine Learning)**in NPTEL- 12 WEEK Course

5.Full Stack python development from MANAC PVT. Limited Hyderabad

**INTERNATIONAL CONFERENCE:**

1. Amrita Kumari & Anil Kumar Sahu “Desiging and Implementation of Linear Feedback shift register and Its Analysis “ Proceeding of 2nd International Conference on Control ,Communication And Computer Technology , ,Bangalore pp.59-65. 19th NOV. CCCT-2011.
2. Anil Kumar Sahu & Pramod Jain, “ Implementation of Pipelined Matrix Multiplier using HDL ” Proceeding of International conference on VLSI design & Embedded Systems Feb 14-16, 2008 (ICVLSI- 08), held at Velammal Engineering College, CHENNAI (INDIA). pp 203-206.

3. Monika singh and Anil Kumar Sahu Presented Paper on “A Survey on Sigma-Delta Analog to Digital Converters” in International Conference “SHAASTRATH” on 23rd -24th March 2014 at Rungta Group of Institutions, Raipur.

4. Anil Kumar Sahu,Vivek Kumar Chandra and Dr. G. R. Sinha “ A Review on System Level Behavioral Modeling and Post Simulation of Built in-Self-Test of Sigma-Delta Modulator Analog-to-Digital Converter” 2nd International Conference on advance and engg. Technology . Anjuman College of Engineering & Technology, Sadar, Nagpur”in   Nagpur 25th and 26 th FEB. 2014. Volume: 3 Issue: 2,paper no. 206-209, ISSN: 2321-8169.

5.Ankita Khurana, Anil Kumar Sahu, Arpit Tiwari, “**Design of Low Power VCO Enabled Quantizer in Continuous Time Sigma Delta ADC for Signal Processing Application”** in IEEE International Conference on Wireless Communication, Signal Processing and Networking (WISPNET), held at SSN College of Engineering Chennai, India during 23rd-25th April 2016, IEEE , VOL 2, ISSUE 1, ISSN 2395-1680, pp.2168-2172, **DOI 978-1-4673-9333-6/16/$31.00.**

6.Arpit Tiwari, Anil Kumar Sahu, Ankita Khurana “**Low Pass Notch Filter Design for Biopotential Signal Acquisition System**”in IEEE International Conference on Wireless Communication, Signal Processing and Networking (WISPNET), held at SSN College of Engineering Chennai, India during 23rd-25th April 2016, IEEE, VOL 2, ISSUE 1, pp. 1491-1495, **DOI 978-1-4673-9333-6/16/$31.00.**

**7**. Y. Tembhre and A. K. Sahu, "Testing of an 8-bit Sigma Delta ADC Based on Code Width Technique Using 45nm Technology," 2016 International Conference on Micro-Electronics and Telecommunication Engineering (ICMETE), Ghaziabad, 2016, pp. 416-420.doi: 10.1109/ICMETE.2016.27

**8**. R. K. Makkad and A. K. Sahu, "Novel design of fast and compact SHA-1 algorithm for security applications," 2016 IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT), Bangalore, 2016, pp.921-925.doi: 10.1109/RTEICT.2016.7807963.

**9.** Anil Kumar Sahu ,Vivek Kumar, Dr. Vivek Kumar Chandra, Dr.G.R.Sinha, “**Design of Single –loop CT Sigma-Delta Modulators for high resolution – wideband applications using GUI"** IEEE ICECDS 2017 Conference Organized in 1st and 2nd Aug in Chennai.

1. Anil Kumar Sahu, Chandrashekhar, Dr. Vivek Kumar Chandra, Dr.G.R.Sinha “**Low Power Op-Amp-less ASDM using 45 nm BICMOS Technology “**IEEE ICECDS 2017 Conference Organized in 1st and 2nd Aug in Chennai.
2. Anil Kumar Sahu, Vivek Kumar Chandra and Dr. G. R. Sinha “ Optimized System Level Modeling of CORDIC Enabled Built-in-Self-Test of Sigma-Delta Analogto-Digital Converter “2017 2nd IEEE International Conference for Convergence in Technology (I2CT)” Pune , 7th -9th April-2017,DOI:978-1-5090-4307-1/17/$31.00 ©2017 IEEE.
3. Anil Kumar Sahu, Vivek Kumar Chandra and Dr. G. R. Sinha “ High Level Computation Technique for Characterization of Sigma-Delta A/D Converter “The**IEEE International Conference on Microelectronics Devices, Circuits and Systems (ICMDCS 2017)** will be held at the VIT University, Vellore India from 10th to 12th August 2017. ICMDCS 2017,DOI: 978-1-5386-1716-8/17/$31.00 ©2017 IEEE.( **Indexed in Scopus**).
4. Rashid Sheikh, Anil Kumar Sahu, “**Ultra Low Power Design Approach of Asynchronous Delta Sigma Modulator “** International Conference on Innovative Research in Science and Technology ICIRST, Published in Scopus Journals(Dec 2017).
5. Sahu A.K., Chandra V.K, and Sinha G. R.2017. *Optimized System Level Modeling of CORDIC Enabled Built-in-Self-Test of Sigma-Delta Analogue-to-Digital Converter*.2nd IEEE. International Conference for Convergence in Technology (I2CT)” Pune **.[Available in IEEE Digital Library]**
6. Sahu A.K., Chandra V.K, and Sinha G. R.2017.*Modeling of Test Stimulus Generator for Characterization of Sigma-Delta A/D using MATLAB/ Simulink*. All India Conference on Digital Technology in electrical and electronic Engineering CSIT Durg ,C.G ,India.(ISBN: 978-81-923288-5-0).
7. Sahu A.K., Chandra V.K, and Sinha G. R. 2017. *High Level Computation Technique for Characterization of Sigma-Delta A/D Converter.*IEEE International Conference on Microelectronics Devices, Circuits, and Systems (ICMDCS 2017) VIT University, Vellore, INDIA.1-4.doi:10.1109/ICMDCS.2017.8211601. **[Available in IEEE Digital Library and also Scopus Indexed]**
8. Sahu A.K., Chandra V.K, and Sinha G. R. 2017. *Design of Single-loop CT Sigma-Delta Modulators for High Resolution -Wideband Applications Using GUI.* IEEE International Conference on energy, Communication, Data Analytic and Soft Computing (ICECDS 2017) .SKR Engineering College Nazarathpet ,Poonamallee, Chennai Tamil Nadu  
   Chennai, India .428-431. **[Available in IEEE Digital Library]**
9. Sahu A.K., Chandra V.K, and Sinha G.R. 2017. *Design of A Low Power Op-Amp-less ASDM using 45 nm BICMOS Technology to linearise VCO-AD*C.IEEE International Conference on energy, Communication, Data Analytic and Soft Computing (ICECDS 2017) . SKR Engineering College Nazarathpet ,Poonamallee,ChennaiTamilNaduChennai, India .241-243.DOI: **[Available in IEEE Digital Library]**
10. Sahu A.K., Chandra V.K, and Sinha G. R.2017.*Modeling and System Level Computer Simulation  Approach for Optimization of Single Loop CT Sigma  Delta ADC.*The International Conference on Data and Information Sciences (ICDIS-2017) .Amerkantak M.P.17-18 November 2017. [**Published in Springer Book Series "Lecture Notes in Networks and Systems”**]. ISBN: 978-981-13-0277-0
11. Sahu, A. K., Chandra, V. K., and Sinha, G. R. 2015. *A Review on System Level Behavioral Modeling And Post Simulation Of Built In-Self-Test Of Sigma-Delta Modulator Analog-To-Digital Converte*r. 2NDInternational ConferenceonAdvances In Engineering & TechnologyNagpur, Maharashtra, India.
12. Sahu A.K., Chandra V.K, and Sinha G. R.2015.*Low Cost Test Generation of Sigma- Delta Analog to Digital Converter for BIST Scheme.* All India Conference on “Sustainable Product Development in Electrical and electronics Engg,CSIT Durg ,5-10. ( ISBN:978-81-923288-3-6).
13. Sahu A.K., Chandra V.K, and Sinha G. R. 2016.*Power optimized Sigma-Delta ADC As DUT for Built-in-Self-Test in 45 Nanometer CMOS*. All India Conference on Clean And Green Technology In Electrical & Electronics Engineering at CSIT Durg.6-12.( ISBN:978-81-923288-4-3).
14. Anil Kumar Sahu, Arvind Kumar Sahu “Low transconductance OTA based active Comb filter for Biomedical Applications” in 2nd International Conference on Advanced Informatics for Computing Research (ICAICR-2018) to be held on July 14-15 2018. **Springer CCIS series (Communications in Computer and Information Science). ISSN Number - 1865-0929**. The books of this series are submitted to ISI Proceedings, EI-Compendex, DBLP, SCOPUS, Google Scholar and Springer Link.
15. Anil Kumar Sahu, Arvind Kumar Sahu “Review of different Filter design techniques and Topologies for Bio-Potential Signal Acquisition Systems” in 3rd IEEE International Conference on Communication and Electronics Systems (ICCES 2018) held on October 15-16, 2018.
16. Anil Kumar Sahu and Ankit Jaiswal  **“MODELLING OF ATTACKS IN SIGMA DELTA ADC FOR HARDWARE SECURITY”** in 3rd International conference on Communication and Electronics System (ICCES 2018).It is **IEEE Conference** held in Coimbatore (India).
17. A. K. Sahu, J. Kumar and R. Tiwari, "Power Computation and Performance Analysis of Viterbi-Decoder Using FPGA," 2020 5th International Conference on Communication and Electronics Systems (ICCES), COIMBATORE, India, 2020, pp. 238-242, doi: 10.1109/ICCES48766.2020.9138087.
18. A. K. Sahu,Abhishek Kumar , "IOT Enabled Hospital Management for Corporate ," 2020 2th International Conference on Data Engineering and Communication Technology (ICDECT) at Kakatiya Institute of Technology & Science (KITSW), Warangal, Telangana, India.[**Scopus Springer Book Chapter**]Accepted and Presented.
19. A. K. Sahu, Neeraj Kumar Misra and Dinesh Kumar "Design of Helath monitoring system for COVID19 pataint” International Conference on Advances in Materials Science, Communication and Microelectronics (ICAMCM-2021). [Accepted and Presented][**IOP Conference Proceeding**]
20. A. K. Sahu, Neeraj Kumar Misra and Dinesh Kumar " Application of Taguchi arrays using DOE for optimising processing and understanding Sputtered coated ZnO TFTs “International Conference on Advances in Materials Science, Communication and Microelectronics (ICAMCM-2021) [Accepted and Presented][**Material Today Proceeding**]
21. A. K. Sahu, Neeraj Kumar Misra and Mounika and Prakash Chandra Sharma “Design and Performance analysis of MIMO Patch Antenna Using CST Microwave Studio” 3rd International Conference on Smart Systems: Innovations in Computing in Manipal University Jaipur. .[**Scopus Springer Book Chapter**].
22. A. K. Sahu, Abhishek Singh and Harish Shakhaya “FILTER DESIGN FOR RADAR SIGNAL ANALYSIS USING FIELD PROGRAMMABLE GATE ARRAY” ICRADMM Amity University Gwalior Campus India .[**Scopus Springer Book Chapter**].
23. P. Asthana, R. K. Kushwaha, A. K. Sahu and N. K. Misra, “Design and Analysis of CMOS based DRAM Cell Structures for High Performance Embedded System in 2 nd International Conference on Micro/Nanoelectronics Devices, Circuits, and Systems (MNDCS-2022) (Virtual Mode), 29-31 Jan 2022. National Institute of Technology Silchar, Assam, India Department of Electronics and Communication Engineering. .[**Scopus Springer Book Chapter**]
24. Anil,Kumar sahu,Abhishek Singh,Sanjay Suman,Bhagyalaxmi “IoT and Cloud Network Based Water Quality Monitoring System Using IFTTT Framework’SVNIT Diamond Jubilee Celebrations Event International Conference on Sustainable Technology and Advanced Computing in Electrical Engineering (ICSTACE) (Virtual) 11th and 12th November 2021, Department of Electrical EngineeringSardar Vallabhbhai National Institute of Technology (SVNIT), Surat, Gujarat- 395007,INDIA**[Scopus Springer Book Chapter**]
25. Anil Kumar Sahu,Rajeev Srivastava ,Preety Verma ,”Architecturae for Health care Process Imporvements using IOE,,AAP Talyer anf Fransic press Book Chapter in Biomedical Engineering and Nanotechnology **[Talyer anf Fransic press Book Chapter**]

**NATIONAL CONFERENCE:**

1. Ashish Tiwari & Anil Kumar Sahu, “An innovative approach of computational fault

Detection using the Design for Testability of CP-PLL” accepted in IEEE National conference on computer and communication systems, NCCCS 2012, 21-22 Nov 2012,

Organized by Dr B. C. Roy Engineering College, Kolkata.

1. Anil Kumar Sahu & Pramod Jain,”Logic BIST controller Architecture for Testing & Diagnosing of Interconnect faults in FPGAs” Proceeding of Nationalconference onEmerging Trends in IT (NCETIT 07) held in SGSITS Indore 18-20, Dec 07 pp 346-50.
2. Anil Kumar Sahu & Pramod Jain, “ Implementation of Pipelined Matrix Multiplier uses HDL ” Proceeding of National conference on Innovation in science & Technology towards Industrial development, Jan 4-5,2008 held at, Rungta Engineering College Bhilai, (C.G.). pp180-185.
3. Anil Kumar Sahu & Amrita Kumari ”implementation of Efficient LFSR ” Proceeding of Nationalconference on (UVRATCH 11) held at SSITM, BHILAI.
4. Anil Kumar Sahu , “ Implementation 3-STAGE PIPELINE MICROCONTROLLER using HDL ” Proceedingof National conference on VLSI design Systems Sep-13, 2011 (MITE VLSI- ), held at MIET ,maureet ,U.P . pp 203-206.

6. Anil Kumar Sahu, Vivek Kumar Chandra and Dr. G. R. Sinha “Improved SNR and ENOB of Sigma-Delta Modulator for Post Simulation and High Level Modelling of Built-in-Self-Test Scheme”National Conference on ‘Application and Electronics for the Welfare of Rural Masses’ 6th and 7th February, 2014, RSR Rungta College of Engineering and Technology, Bhilai.

7.Zeesha Mishra and Anil Kumar Sahu Published paper titled **“A review on architecture of high speed data communication for USB 2.0 device using FPGA”** in National Conference on Application of Computer and Electronics for the Welfare of Rural Masses, held on 6TH – 7TH Feb 2015.

8. Zeesha Mishra and Anil Kumar Sahu Published paper titled **“Transceiver Microcell Architecture of USB 2.0”** in 13th Chhattisgarh Young Scientists Congress-2015, held on Indra Gandhi Krishi Vishwavidyalaya, Raipur on 28th Feb – 1st March 2015.

9. Zeesha Mishra and Anil Kumar Sahu Published paper titled **“Hardware Efficient Transceiver Microcell Architecture of USB 2.0 for High Speed data Communication using FPGA”** in CiiT international Journal 2015 Volume 7.

10. Anil Kumar Sahu, Vivek Kumar Chandra and Dr. G. R. Sinha “ DESIGN OF CONTINUOUS TIME SIGMA DELTA ADC FOR SIGNAL PROCESSING APPLICATION”, National Conference On Signal Processing, Sustainable Energy Materials And Astronomy And Astrophysics (Nssema -2017) March 28-30, 2017 Sos In Electronics & Photonics And Sos In Physics & Astrophysics Pt. Ravishankar Shukla University, Raipur, 492010, (C.G) India.

11.Sahu A.K., Chandra V.K, and Sinha G. R. 2015.*Improved SNR and ENOB of Sigma-Delta Modulator for Post Simulation and High Level Modeling of Built-in-Self-Test Scheme.* In National Conference of Applications of Computers and Electronics for the Welfare of Rural Masses, at RSR - Rungta College of Engineering & Technology, Bhilai.

12.Sahu A.K., Chandra V.K, and Sinha G. R. 2017. *Design Of Continuous Time Sigma Delta ADC For Signal Processing Application*. National Conference On Signal Processing, Sustainable Energy Materials And Astronomy And Astrophysics (Nssema -2017), Sos In Electronics & Photonics And Sos In Physics & Astrophysics Pt. Ravishankar Shukla University, Raipur, 492010, (C.G) India.

**Annexure- 5**

**Paper Published in International & National Journals**

1. Ashish Tiwari, Anil kumar Sahu & Dr. G. R. Sinha, “Design for testability architecture

Using existing elements of the CP-PLL for Digital Testing Applications in VLSI ASIC

Design” published in “International journal of VLSI and Signal Processing Applications”, volume 2 issue 1, Feb 2012, (56-64), ISSN 2231-3133.

1. Ashish Tiwari, Anil kumar Sahu & Dr. G. R. Sinha, Dr. V. K. Chandra, “A novel approach of stimulus generation and measurement for BIST in CP-PLL testing scheme” selected in the best paper category in “International journal of Computer Science and Information Security”, volume 10 issue 2, Jan 2012, ISSN 1947-5500.
2. Ashish Tiwari & Anil Kumar Sahu, “Mixed Signal IC (CP-PLL) Testing scheme using a novel approach” published in “International Journal of Scientific & Engineering Research”, Volume 3, Issue 5, May-2012, ISSN 2229-5518.
3. Darshana Dongre, Anil Kumar Sahu “ Implementation of AXI Design core with DDR3 memory controller for SoC “ISSN 2249-6343 International Journal of Computer Technology and Electronics Engineering (IJCTEE) Volume 1 , Issue 3,2011.
4. International Journal of Computer Technology and Electronics Engineering (IJCTEE) Volume 1, Issue 3, ISSN 2249-6343“Implementation of AXI Design core with DDR3 memory controller for SoC ”.
5. Sangita Shit Anil Kumar Sahu “Design and Analysis of LINAC Control System in FPGA” International Journal of Computer Technology and Electronics Engineering (IJCTEE) Volume 2, Issue 139, ISSN 2249-6343.
6. Priyanka Bibay, Anil Kumar Sahu, Dr. Vivek Kumar Chandra, “Design and Implementation of DDR SDRAM Controller using Verilog” in the ‘International Journal of Science and Research (IJSR)’, ISSN: 2319 7064, Volume 2, Issue 1, pp. 320-324, January 2013.
7. Priyanka Bibay, Anil Kumar Sahu, “RTL Design of DDR SDRAM Controller Using Verilog”, in the ‘International Journal of Engineering Research & Technology (IJERT)’, ISSN: 2278 0181, Volume 1, Issue 10, pp. 1-4, December 2012.
8. Priyanka Bibay, Anil Kumar Sahu, “Optimized Design and Simulation of DDR SDRAM Controller Using Verilog” in the journal of International Conference Shaastrarth 2013 – ‘International Conference On Eco Friendly Technologies in Electronics & Telecommunication for Sustainable Growth’, February 2013.

10. Rajeev Kumar Singh, Anil Kumar Sahu, Dr. Vivek Chandra ” Design and Implementation of Discrete Cosine Transform Architecture Blocks”, in proceeding of Shaastrath, An International Conference Rungta College of Engg. And Technology, Bhilai, 8th and 9th February 2014.

11. Published paper Titled “Resetting 2-Order Sigma –Delta Modulator in130 nm CMOS Technology” in International Journal of Advanced Research in Computer Engineering & Technology (IJARCET) Volume 3 Issue 7, July 2014 2429 ISSN: 2278 – 1323.

12. Akanksha Pawar, Anil Kumar Sahu, Dr. G. R. Sinha. (Vol. 3 - Issue 11 (November - 2014)). " *Implementation of LMS Adaptive Filter using High Speed Vedic Multiplier* ", International Journal of Engineering Research & Technology (IJERT), ISSN: 2278-0181, www.ijert.org

13.Akanksha Pawar, Anil Kumar Sahu, Dr. G. R. Sinha. (Vol. 1 - Issue 10 (November - 2014). " *Implementation of High Speed Vedic Multiplier* ", International Journal of Innovative Research in Advanced Engineering (IJIRAE) ISSN: 2349-2163, <http://www.ijirae.com/>

14.Archana Fande, Anil Sahu, “Efficient Implementation & Comparison of Signed Complex Multiplier on FPGA using FFT Algorithm”, In International Journal of Scientific Research, Engineering & Technology, (IJSRET), May-2014, ISSN:2278-0882.

15.Anil Kumar Sahu, prateek verma,,Dr.Vivek Kumar Chandra,Dr,G. R. Sinha “A Graphical User Interface Implementation of Second Order Sigma- Delta Analog to Digital Converter with Improved Performance Parameters”, In International Journal of Scientific Research, Engineering & Technology, (IJSRET), July-2014, ISSN:2278-0882.

16. Monika Singh and Anil Kumar Sahu Published Paper titled”SNR Reduction of 2nd order Sigma-Delta Modulator Using Genetic Algorithm” in the International Journal Of Digital Application & Contemporary Research (IJDACR), Vol.3, Issue12, September 2014, ISSN: 2319-4863.

17.Anil Kumar Sahu and Bhawesh Sahu “FPGA Implementation of IP-core of FFT Block for DSP Applications, ” International Journal of Innovative Science, Engineering & Technology, Vol. 1 Issue 10, page no. 498-503, December 2014 .ISSN 2348 – 7968.

18.Anil Kumar Sahu and Bhawesh Sahu “Design & Development of IP-core of FFT for Field Programmable Gate Arrays.” International Journal of Innovative Research in Advanced Engineering (IJIRAE) ISSN: 2349-2163 Volume 1 Issue 8, page no. 233-239. (September 2014).

19. Anil Kumar Sahu, Vivek Kumar Chandra and Dr. G. R. Sinha “ A Review on System Level Behavioural Modelling and Post Simulation of Built in-Self-Test of Sigma-Delta Modulator Analog-to-Digital Converter” International Journal on Recent and Innovation Trends in Computing and Communication Volume: 3 Issue: 2, page no. 206-209, ISSN: 2321-8169.(2014).

20. Anil Kumar Sahu, Vivek Kumar Chandra and Dr. G. R. Sinha “Improved SNR and ENOB of Sigma-Delta Modulator for Post Simulation and High Level Modelling of Built-in-Self-Test Scheme”on *International Journal of Computer Applications* Volume: -- Issue:, page no--.  *. ISSN: (0975 – 8887). Communicated in final print.*

1. Zeesha Mishra and Anil Kumar Sah Published paper titled ***“A review on architecture of high speed data communication for USB 2.0 device using FPGA”*** in International Journal of Computer Application (IJCA) 0975-8887 published.
2. Akansha Sahu and Anil Kumar Sahu Published Paper titled **“A Review on Multiplier based on Reversible Logic Gate and Vedic Algorithm for Quantum Computing”** inInternational Journal of Engineering Research & Technology (IJERT)Volume. 4, Issue. 04, April 2015, pp-992-994, ISSN:2278-0181.
3. Akansha Sahu and Anil Kumar Sahu Published Paper titled **“ Design of High Speed 64x64 Bit Fault Tolerant Reversible Vedic Multiplier”** inInternational Research Journal of Engineering & Technology(IRJET) Volume 2, Issue 3, June 2015, pp-850-887 ISSN:2595-0056.
4. Akansha Sahu and Anil Kumar Sahu Published Paper titled **“High Speed Fault Tolerant Reversible Vedic Multiplier ”** inInternational Research Journal of Engineering & Technology(IJIRAE) Volume 6, Issue 6, June 2015, pp-71-78 ISSN:2349-2163.
5. Akansha Sahu and Anil Kumar Sahu Published Paper titled “title **“ Design of 4x4 Parity Preserving Reversible Vedic Multiplier”** inInternational journal of Advanced Engineering Research & Technology, Volume 3,Issue 4 April-May 2015,pp-153-158 ISSN No: 2348 – 8190.
6. Akansha Sahu and Anil Kumar Sahu Published Paper titled **“Design of 64x64 Bit Parity Preserving Reversible Vedic Multiplier Using Carry Look Ahead Adder”** inCoimbatore Institute of Information Technology International Journal, June 2015 (Accepted).
7. Jageshwar Prasad Sinha1, Anil Kumar sahu2, “NEW EFFICIENT REDUDANT RADIX 4 MULTIPLIER DESIGN USING VHDL” International Journal of Multidisciplinary Research and Development, Volume: 2, Issue: 5, 258-262 May 2015 www.allsubjectjournal.com e-ISSN: 2349-4182 p-ISSN: 2349-5979 Impact Factor: 3.762.
8. Jageshwar Prasad Sinha1, Anil Kumar sahu2 “An Efficient Approach of Coprocessordesign using RR4 Algorithm” International Journal of Multidisciplinary Research and Development. Volume: 2, Issue: 5, 263-269 May 2015 www.allsubjectjournal.com e-ISSN: 2349-4182 p-ISSN: 2349-5979 Impact Factor: 3.762

29.Ankita Khurana, Anil Kumar Sahu, “**Design of Low Power VCO Enabled Quantizer in Continuous Time Sigma Delta ADC for Signal Processing Application”** in ICTACT journal on Micro-Electronics (IJMT), held at Chennai, April-2016, VOL.2, ISSUE 1, and ISSN 2395-1680.

30.Ankita Khurana, Anil Kumar Sahu, “**A fourth order 1. 8V Power Supply Loop Filter in Continuous Time Delta-Sigma ADC implemented in 0. 18-um CMOS Technology**” in Coimbatore Institute of Information Technology International Journals (CIIT), held at Chennai, April-2016, VOL 8, ISSUE 4, ISSN 0974-9594.

31.Arpit Tiwari, Anil Kumar Sahu,“**Design of Low Transconductance OTA for Biopotential Signal Acquisition System**” in **International Journal of Advanced Research in Electrical, Electronics AND Instrumentation Engineering** (IJAREEIE) Vol. 4, Issue 11, November 2015 pp. 9315-9321 ISSN (Online): 2278-8875, ISSN (Print): 2320-3765.

32.Arpit Tiwari, Anil Kumar Sahu,“ **Low Noise Elliptical Filter in 250 Nanometre for EEG Signals” in Coimbatore Institute of Information Technology**  **International Journals (CIIT)** Vol. 8 No.5 May 2016 pp. 126-129.

35. Yogita and Anil Kumar Sahu “A Code Width, Built in Self-Test Circuit for Eight Bit Sigma Delta ADC” in Coimbatore Institute of Information Technology International Journals (CIIT). Volume 4, April 2016.

36. Yogita and Anil Kumar sahu“Implementation of 8-bit Sigma-Delta ADC using 45nm Technology” In International Journal For Research In Applied Science And Engineering Technology (IJRASET).

37. Vivek Kumar, Anil Kumar Sahu “**A Review on Continuous Time Sigma Delta Modulator**” International Journal of Scientific Research (IJSR) Vol-6, Issue-6, June 2017, ISSN NO 2277-8179, IF: 4.176, IC Value: 78.46**.** **(UGC Approved Journal).**

**38.** Chandrashekhar, Anil Kumar Sahu “**A Review on linearize VCO-ADC**” International Journal of Scientific Research (IJSR) Vol-6, Issue-6, June 2017, ISSN NO 2277-8179, IF: 4.176, IC Value: 78.46. **(UGC Approved Journal).**

**39.** Mr. Rashid Sheikh, Mr. Anil Kumar Sahu “A Short Survey on Low Power Asynchronous Delta Sigma Modulator” IOSRAT Journal of VLSI and Signal Processing (IOSRAT-JVSP) ISSN: 2278-2834 Volume 1, Issue 2 (Feb 2017), PP 01-05 www.iosrat.org.

**40.**Rashid Sheikh, Anil Kumar Sahu, “**A Study on 0.25-V 28-nW 58-dB Dynamic Range Asynchronous Delta Sigma Modulator in 130-nm Digital CMOS Process "** IOSRAT Journal of VLSI and Signal Processing (IOSRAT-JVSP) ISSN: 2278-2834 Volume 7, Issue 2 (June 2017).

**41.** Sahu, A. K., Sheikh, R., & Surendar, A. (2017). Ultra low power design approach of asynchronous delta sigma modulator. *International Journal of Engineering & Technology*, *7* (1.1), 84-87. (**Scopus Index Journal**)

42. Anil Kumar Sahu, Ankit Jiaswal. “Detection of hardware trojans for mixed signal hardware security: A REVIEW in Special Issue of Journal of Advanced Research in Dynamical and Control Systems. Vol. 9 Issue 14/2017 .Page no. 2739-2754.ISSN: 1943-023X. (**Scopus Index Journal**)

43. Sahu A.K., Chandra V.K, and Sinha G. R. 2014.*A Review on System Level Behavioural Modelling and Post Simulation of Built -in –Self- Test of Sigma-Delta Modulator Analog-to-Digital Converter*. International Journal on Recent and Innovation Trends in Computing and Communication.3 (2): 206-209. ISSN No.: 2321-8169.

44.Sahu A.K., Chandra V.K, and Sinha G. R. 2014.*A Graphical User Interface Implementation of Second Order Sigma- Delta Analog to Digital Converter with Improved Performance Parameters.* In International Journal of Scientific Research, Engineering & Technology, (IJSRET). 2(7):104-110. ISSN No.: 2278-0882.

45.Sahu A.K., Chandra V.K, and Sinha G. R. (2015). *Improved SNR and ENOB of Sigma-Delta Modulator for Post Simulation and High Level Modelling of Built-in-Self-Test Scheme.* In International Journal of Computer Applications. (ACEWRM). 3:11-14. **[EBSCO Index]**

46. Sahu A.K., Chandra V.K, and Sinha G. R. 2015.*System Level Behavioural Modelling of CORDIC Based ORA of Built-in-Self-Test for Sigma-Delta Analog-to-Digital Converter*. In International Journal of Signal and Image Processing, Infinity Sciences Issues. 1:37-44. ISSN No.: 2458-6498.

47.Sahu A.K., Chandra V.K, and Sinha G. R. 2016. *A 6.7mW   8-bit Power optimized Sigma-Delta ADC As DUT for Built-in-Self-Test in 45nm CMOS*. In **CIIT Journal** of Programmable Device Circuits and Systems. *8* (2): 121-127.**Print: ISSN No.: 0974 – 973X & Online: ISSN No.: 0974 – 9624.** [ **UGC Unpaid Journal**]

48.Sahu, A. K., Chandra, V. K., and Sinha, G. R. 2017. *Optimized system level design and simulation analysis for characterization of performance of single loop CT sigma-delta modulators A/D*. International Journal Of Engineering Sciences & Research Technology, 6 (9): 249-254. ISSN No.: 2277-9655. [**UGC Journal**]

49.Sahu, A. K., Chandra, V. K., and Sinha, G. R. 2017. *Design of Continuous Time Sigma Delta ADC for Signal Processing Application*. International Journal Luminescence and application, 7 (3-4): 486-490. ISSN No.: 2277-6362.

50.Sahu, A. K., Chandra, V. K., and Sinha, G. R. 2017. *System Level Modelling and Simulation of Built-in-Self-Test Enable Oversampling Analog-to-Digital Converter*. The Asian Journal of Convergence of Technology (AJCT), ISSN No.: 2350-1146, I.F 2.71Volume III, Issue III, 2017. https://doi.org/https://doi.org/10.1212/ajct.v3i3.316. [**UGC Unpaid Journal**]

51.Sahu A.K., Chandra V.K, and Sinha G. R.2017. *Coordinate Rotation, Digital Computer Enabled* Knowledge in Engineering and Technology in International Journal of Pure and Applied Mathematics.117 (15): 465-477.ISSN No.: 1311-8080 (printed version); ISSN No.: 1314-3395 (on-line version). [**Scopus Index and UGC Approve Journal**].

<http://acadpubl.eu/jsi/2017-117-15/issue15.html>.

52.Sahu A.K., Chandra V.K, and Sinha G. R.2017.*Modeling And Analysis Of Quantization Noise And Power Estimation Of Continuous-Time Delta Sigma Analog-To-Digital Converter Using Test Enable Feature For 4G Radios*. Special Issue On Environment, Engineering & Energy in Journal of Advanced Research in Dynamical and Control Systems.9 (14): 1323-1333.ISSN No.: 1943-023X. [**Scopus Index and UGC Approve Journal**].

<http://www.jardcs.org/abstract.php?archiveid=1899>.

*Built-in-Self-Test Scheme for Oversampling Analog-to-Digital Converter*. Special Issue On Recent

53.Sahu A.K., Chandra V.K, and Sinha G. R.2018. *Design Concept of Reduction of Chip Area Overhead and Power Consumptions of Single Loop CT Sigma Delta ADC Using BIST*. 31 March 2018 Special Issue (Emerging Engineering Technologies, Trends) in **Journal of Engineering Technology.** 6:174-188.ISSN: 0747-9964. [**Science Citation Index Expanded, Scopus Index and UGC Approve Journal].**

54.Sahu A.K., Chandra V.K, and Sinha G. R. 2016. *Modelling of Test Stimulus Generator and CORDIC Logic for Testing of CT Sigma Delta Analog-To-Digital Converter*. In **CiiT International Journal of Fuzzy Systems**. **Print: ISSN No.: 0974 – 9721& Online: ISSN No.:** **0974 – 9624.** [ **UGC Unpaid Journal**]

55.Sahu A.K.,Soni Sapna.2017. *A Review on Design and Implementation of Sigma Delta Converter for Neural Recording*.Special Issue On Recent Knowledge in Engineering and Technology in International Journal of Pure and Applied Mathematics.117(21):621-630.ISSN No.: 1311-8080 (printed version); ISSN No.: 1314-3395 (on-line version). [**Scopus Index and UGC Approve Journal**].

<http://acadpubl.eu/jsi/2017-117-20-22/articles/21/54.pdf>

56. Anil Kumar Sahu , Swati Singh Solanki “ULTRA LOW POWER CONSUMING VLSI ARCHITECTURE FOR MONTGOMERY MODULAR MULTIPLIER USING ADIABATICARRAY LOGIC” Journal of Advance Research in Dynamic and Control system (JARDCS) ,ISSN 1943-023X,Special Issue-06,2018,page756-765.[**SCOPUS JOURNAL**]

57. SINGH SOLANKI, Swati; SAHU, Anil Kumar. Power-Efficient Montgomery Modular Multiplication Review Using VLSI Architecture. Programmable Device Circuits and Systems, [S.l.], v. 10, n. 6, p. 108-112, Jun. 2018. ISSN 0974 – 9624. Available at: <http://www.ciitresearch.org/dl/index.php/pdcs/article/view/PDCS062018002.>. Date accessed: 02 Nov. 2018.

58 Dr. Anil Kumar Sahu ; Vivek Kumar Chandra ; G R Sinha ; Neeraj Kumar Misra “An Efficient CTDSM Based On GM-C Quantizer and Improved Dynamic Element Matching”Published MANUSCRIPT **in IET Circuits, Devices & Systems**, 7 pp. DOI: 10.1049/iet-cds.2019.0404 , Print ISSN 1751-858X, Online ISSN 1751-8598.[**SCI** **Journal**]

59. Dr. Anil Kumar Sahu ; abhilasha Sigrole “ A FPGA Approach of Coprocessor Designing Using RR4 Algorithm” in journal of TEST Engineering & Management January - February 2020 ,ISSN: 0193 - 4120 Page No. 11186 – 11190.[**SCOPUS JOURNAL**]

60. Dr. Anil Kumar Sahu ; Jiendra Kumar , Ravi Tiwari “High Performance Veterbi decoder using FPGA” in Internal reserech of journal of modernization in Engg. Trechnology and Science – April 2020 ,ISSN: 2582-5208 ,Vol.2,issue 4 ,Page No. 1 – 7.

61. Yadav, Om Prakash, and Anil Kumar Sahu. "Electrocardiogram estimation using Lagrange interpolation." **IET Electronics Letters**. Electronics Letters Current Issue Online ISSN 1350-911X Print ISSN 0013-5194 [**SCI** **Journal**]

[**https://doi.org/10.1049/ell2.12041**](https://doi.org/10.1049/ell2.12041)

62. Paranjape, V., Nihalani, N., Sahu, A. K., & Shakya, H. K. (2020). Clustering Based Customer Segmentation Using Automatic Billing System for Smart Shopping. *Solid State Technology*, *63*(6), 7273-7293. ISSN **0038-111X** (online) [**SCOPUS JOURNAL**]

63. Goud, H., Swarnkar, P., Shankar, V. G., & Sahu, A. K. (2021). A Comparative Analysis of Conventional PID Tuning Techniques for Single Link Robotic Arm. Solid State Technology, 64(2), 565-574. ISSN **0038-111X** (online) [**SCOPUS JOURNAL**]

64. Anil Kumar Sahu, Vivek Kumar Chandra & G. R. Sinha ,Economic Modelling and Implementation of Test Signal Generator for Characterization of Continuous Time Sigma-Delta Analog-to-Digital Converter in Radioelectronics and Communications Systems volume 62, pages241–250 (2019**)**  ISSN **1934-8061** (Online), ISSN 0735-2727 (Print) **.**

**[Scopus Index Journal]**

65. Anil Kumar Sahu, Arram Sriram, G. Sekhar Reddy, G. L. Anand Babu, Prashant Bachanna,Singh Chhabra Gurpreet,Vishal Moyal, D. C. Shubhangi, Devanand Bhonsle,R. Madana Mohana, K. Srihari “A Smart Solution for Cancer Patient Monitoring Based on Internet of Medical Things Using Machine Learning Approach” In **Hindawi Journal of Evidence-Based Complementary and Alternative Medicine** / 2022 / Article. Volume 2022 |Article ID 2056807 | https://doi.org/10.1155/2022/2056807. ISSN: 1741-427X (Print)ISSN: 1741-4288 (Online)

[**SCI** **Journal**] Impact Factor **2.650**

66. Anil Kumar Sahu, Arram Sriram, G. Sekhar Reddy, G. L. Anand Babu, Prashant Bachanna, Shubhangi,Anil Kumar Sahu, Devanand Bhonsle,R. Madana Mohana, K. Srihari “Anteena Design for Spectrum Sharing in 5G wireless sysem ” In **Hindawi Journal of** Wireless Communications and Mobile Computing ISSN:1530-8669(Print)ISSN:1530-8677(Online).[**Accepted**]

[**SCI** **Journal**] Impact Factor **2.140**

**TOTAL NO. OF RESEARCH PUBLICATIONS** = 113

( International Journal = 66; National & International Conferences = 47)

**TOTAL NO. BOOKS 3**

**1.Editor of Book** A Low Power Discrete Time Band-Pass Sigma Delta Modulator ADC 6203931292 First Editor/One of the Two Editor Lambert Academic Publishing

**2.Editor of Book**  A Low Power LNA design

6203931296 First Editor/One of the Two Editor Lambert Academic Publishing 2021 International

**3.Editor of Book**  :Fundamental of Machine Leaning with ISBN NO. 978-93-91265-33-5 LAMBERT PUBLICATION’S

**PATENT LIST –PUBLISHED AND GRANTS**

**PATENT LIST –PUBLISHED**

**1.TITLE:** ITMD-DEVICE: INTELLIGENT TECHNOLOGY TO MAXIMIZE THE

DISPLAY AREA OF A MOBILE DEVICE

**APPLICATION NUMBER:** 202011009101

**PUBLICATION DATE (U/S 11A) :** 20/03/2020

**2.TITLE:** RWO-MOBILE CACHE MEMORY: ADVANCED TECHNIQUES READ AND

WRITE OPERATIONS ON MOBILE CACHE MEMORY.**APPLICATION NUMBER:** 202011006936**PUBLICATION DATE (U/S 11A) :** 28/02/2020

**3.TITLE:** IPCPC-VLSI-CIRCUITS: INTELLIGENT PROCESS OF COMPUTING DUAL-CONDUCTOR PARASITIC ADVANCED CAPACIT ANCES FOR VLSI CIRCUITS.**APPLICATION NUMBER:** 202041006276**PUBLICATION DATE (U/S 11A) :** 21/02/2020

**4.TITLE:** INTELLIGENT METHOD TO INCREASING AIR CONDITIONER

PERFORMANCE AND DECEASING MAINTENANCE.**APPLICATION NUMBER:** 202011007757

**PUBLICATION DATE (U/S 11A) :** 06/03/2020

**5. TITLE:** DISINFECTS CLOTHES, EA TING FOOD, VEGET ABLE, FRUIT , JUICE,

GROCERIES, KITCHEN ITEMS USING ULTRAVIOLET LIGHT**APPLICATION NUMBER:** 202041028746

**PUBLICATION DATE (U/S 11A) :** 06/07/2020

**6.** **TITLE:** CREDIT CARD FARUD PREVENSION : INTELLIGENT PROCESS TO

CREDIT CARD FRAUD PREVATION USING MACHINE LEARNING

**APPLICATION NUMBER** : 202041033789

**PUBLICATION DATE (U/S 11A**) : 16/08/2020

**PATENT LIST –GRANTS**

**1.** **TITLE:** LMS quqntum Computing :Large database base stored in to small memory using qutanum computing and AI Based Programming

**APPLICATION NUMBER** : 2020102068

**PUBLICATION DATE (Ausrtralian-Granted )** : 1/9/2020

**2.** **TITLE:** Intelligent Plug and Play Point to Multipoint Internet of Things (loT) Platform and

Method of Managing the Same

**APPLICATION NUMBER** : AU 2021103479 A4

**PUBLICATION DATE (Ausrtralian-Granted** ) :21/04/2022

**PROJECT GRANTS:**

**1.SPICE Projects under AICTE for Two Year**

Scheme for Promoting Interests, Creativity & Ethics among Students (SPICES) Team

Institutional Development Cell

All India Council for Technical Education, New-Delhi

Amount : 2 Lakhs

F.N o. 1 0- 46 / ATCTE/I DCISPI CES 12020-21

CO-PI : Dr Anil Kumar Sahu

PI: Dr. Papiya Dutta

Status: COMPLETED

**AI AND ML BASED PROJECT AND CASE STUDY:**

1. HUMAN POSE ESTIMATION USING MACHINE LEARNING IN PYTHON
2. Child Abuse content detection on the web using python.
3. Detection of Fake Images using Machine Learning .
4. A Deep learning based Architecture to Diagnose Diabetes using Retinal Images only
5. Fake user detection for social media applications using machine learning in python
6. Driver's Drowsiness Monitoring System using Visual Behaviour and Machine Learning.
7. Case study on Statical Concept like P-Test ,T-test,Z test,distribution in predictive analysis
8. Case study on Classification problem Machine Leaning using ML model,XgBoost,Random forest,Cross validation and Performance Analysis.(PCA ,Confusion Matrix,ROCAUC,Model Accuracy 99% etc
9. Case study on Regression problem Machine Leaning using logistic Regression ,XgBoost,Random forest,Cross validation and Performance Analysis, Model Accuracy 99%.
10. Case Study based on NLP and Deep leraning Model
11. Case study of YOLO model,RNN,CNN object Detection.

**PROFESSIONAL MEMBERSHIP:**

1. **South Asia Institute of Science and Engineering (SAISE).**Membership No.: 20180323001.
2. **International Association of Engineer (IAENG )**

Membership No.: 212666.

1. **MIR Labs (Machine Intelligence Research Labs)**

**Regular Membership**

**Member Id :694 .Member Since : Nov 2018.**

1. **IETE Fellow Membership for Life time:F-502151**
2. **International Journal of Innovative Research in Engineering and Multidisciplinary Physical Science.**
3. **Awards**
4. Best paper awrad in 2 nd International Conference on Micro/Nanoelectronics Devices, Circuits, and Systems (MNDCS-2022) (Virtual Mode), 29-31 Jan 2022. National Institute of Technology Silchar, Assam, India Department of Electronics and Communication Engineering

Paper # 33: P. Asthana, R. K. Kushwaha, A. K. Sahu and N. K. Misra, “Design and Analysis of CMOS based DRAM Cell Structures for High Performance Embedded System”.

1. Secured Second Postion in Top 10 runnerup in IBM international Idea Hackhthon 2020.

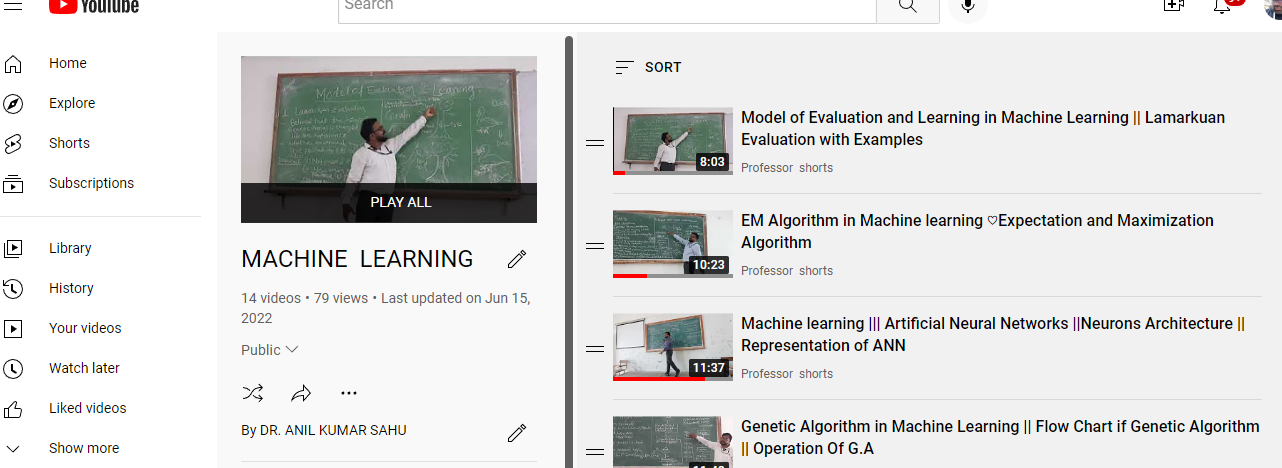
**REVIEWER**

1. Reviewer of IEEE International Conference on Electronics, Circuits and Systems 9-12 December 2018, Bordeaux, France.
2. Reviewer of Springer Journal of Design Automation for Embedded Systems (DAEM) .
3. [Reviewer of Journal of Computer Science · Science Publications.](https://thescipub.com/journals/jcs)
4. [Reviewer of Estimating Thermal Noise in ΔΣ ADCs Composed of Switched Capacitor Integrators" for the IEEE Transactions on Circuits and Systems II: Express Briefs.](https://thescipub.com/journals/jcs)
5. [Reviewer of International Journal of Public Sector Performance Management (IJPSPM) In Inderscience Journal.](https://thescipub.com/journals/jcs)
6. Reviewer of International Journal of Technology Intelligence and Planning (IJTIP) in Inderscience Journal.

**MAJOR CONTRIBUTION AS ASSOCIATE PROFESSOR**

1. Improved image of the college through academic Performance on Results of CSVTU .
2. Contribution on Accredation of four BTech Engg programmes (ECE ) from NBA and NAAC body.
3. Best Faculty award in BIET.
4. Traing Incharge For Placements.
5. Project Incharge College Level.
6. Convenor of organized Conference ,Seminor,FDP and Workshops.
7. Highest Reserch activities annually.
8. IIC Ambessdor in BIET
9. Top You Tube Creater ICT Lecturer of Machine Learning ,Artifical Intellegent and Microwave communication Eneginnering etc.
10. AIIRA Incharge of BIET

<https://youtube.com/playlist?list=PLvPcoW4xsdq5w3wtoas9hR7AcNTYD2O9m>



**ANNEXURE-6**

**ONE PAGE STATEMENT AS TO WHY SHOULD BE SELECTED**

1. Multi faced experiences in research, teaching.
2. Believes in the Performance index which is applicable for Faculty, Staff and Students based on Teaching learning Process, consultancy services, Research and Development work, innovative idea exchange programmers from renowned institutes and also through organizing continuing education programmed.
3. Believes in utilization of available resources.
4. Vast experience of developing Labs.
5. Worked in various places having different cultural habitats, this will help me to have social coordination with any unknown society.

**Name & Address of Referees:**

1. Dr. Mahendra Shakre

Assistant Professor ,ECE,IIIT Ropar(Panjab)

1. Dr. G.R.Sinha,

Adjunct professor,IIIT Banglore,India

**DECLARATION:**

It is certify that the above particulars submitted are true to the best of my knowledge.

Date:

Place:

(Signature of the Candidate)