Cross-linked poly-vinyl phenol based bilayer dielectrics: its importance and applications in electronic devices

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Abstract :

Poly-vinyl phenol (PVP) is one of the chosen polymer which finds tremendous applications in the fabrication of electronic devices. One of the major area of applications of PVP is in the development of gate dielectric material for organic thin film transistors (OTFTs). In this chapter, we report on the synthesis and characterization of cross-linked PVP (cPVP)and modified cPVP gate dielectrics using an organic-organic fabrication approach. Electrical properties of the resultant devices are reported.

Keywords: Poly-vinyl phenol, gate dielectric, thin film transistor.

Contents:

1. Overview of polymer based bilayer gate dielectrics in OTFT applications
2. Synthesis of cPVP dielectric films based MIM and OTFT
3. Characterization of the dielectric films
4. Electrical properties of the cPVP based OTFTs
5. Conclusion
6. Future recommendations

**1. Overview of polymers based bilayer gate dielectrics in OTFT applications**

Organic thin-film transistors (OTFTs) are now making significant progress into many large-area applications, considering its advantages, such as low cost, lightweight and possible fabrication on the flexible substrate as well as of its large-area feasibility. A thin-film-transistor (TFT) is an insulated-gate field-effect transistor consisting of thin films of metal, insulator, and semiconductor whose operation depends on the same basic principle as a metal oxide semiconductor field-effect transistor (MOSFET) [1-5]. Nowadays researchers are more interested in the organic electronic devices [2-3, 6-9]. Light emitting diodes, organic thin film transistors, solar cells, etc. are the few examples. The gate dielectrics play a major role in the successful commercialization of OTFTs. The development of bilayer gate dielectric materials based on organic-organic, organic-inorganic, inorganic-inorganic approaches have made revolutionary improvement in the performance of OTFTs. Different polymers are used in the fabrication of dielectric materials. Poly-vinyl alcohol (PVA), poly-vinyl phenol (PVP), poly-methyl methacrylate (PMMA) are some polymers which find wide applications as gate dielectrics in OTFTs. The suitability of the gate dielectric materials in OTFTs is based on parameters like, high capacitance, high dielectric constant and low leakage current. The flexibility of the gate dielectric is also considered for fabrication of smart devices. Peng et al. in 1990, reported the use polymeric organic materials as gate dielectrics in OFETs fabricating devices with a variety of organic polymer dielectrics resulting a relationship between the field-effect mobility and the dielectric constant [10]. One of the significant bilayer hybrid dielectric development came in the form of PMMA/Ta2O5 [11]. The Ta2O5 layer was thermally deposited on ITO glass followed by the deposition of a second layer of PMMA using a spin coater, on the top of the first layer. The OTFT device performance was estimated at varying thickness values of PMMA layer. After a series of experiments the research group of Tardy had optimized the dielectric thickness at 37 nm and accordingly devices were fabricated by them and characterized. Pentacene was used as the semiconductor in PMMA/Ta2O5 dielectric based OTFT. The performance of the PMMA/Ta2O5 dielectric based OTFT was also compared to an OTFT device with single layer dielectric of Ta2O5. The bilayer devices resulted in an increase in the ionic mobility and the Ion-off ratio making the bilayer dielectric based OTFT superior to the single layer OTFT. In continuation to their earlier work on PMMA/Ta2O5, Tardy et al further progressed and deposited Ta2O5 using electron beam evaporation. The current mobility and the Ion-off ratio had further improved compared to their work on thermally deposited Ta2O5 layer [12-13]. The work of Tardy et al has propelled the OTF research using bilayer dielectrics. Bilayer dielectrics of cPVA-SiO2 was fabricated and characterized. The silica layer was deposited using plasma mediated CVD technique and cross-linked PVA (cPVA) was spin coated on the top of it. This device resulted in very low hysteresis making it suitable for electronics [14]. The researchers of this work had attributed the performance of their devices to the thickness of both the dielectric layers. The optimized dielectric layer thickness was found to be 350 Å and 950 Å for silica and cross-linked PVA respectively. The possible explanations for the observed low hysteresis with silica-cPVA dielectric layer was the less trap density at the electrode-dielectric interface. The current mobility for the silica-cPVP device was recorded to be 0.12 cm2V-1s-1 which was superior to the single layer silica device as explained in the work. One of the acceptable explanation for the enhanced current mobility could be the high dielectric constant (high k) values of cross-linked poly-vinyl alcohol. The leakage current was estimated to be low probably due to the deposition of the cross-linked PVA layer on top of silica layer. As a result of this, the Ion-off ratio had also improved to 2 × 106. The stability of the OTFT devices are critical factor for commercialization. The OTFT device with the bilayer gate dielectric i.e. silica-cPVA was found to be more stable at ambient atmosphere and on applied bias stress compared to the single layer silica device. Inspired by these development in bilayer dielectric OTFTs, Im and his co-workers developed poly-vinyl phenol (PVP) and Yettrium oxide based hybrid gate dielectrics [15]. The have also used pentacene as the semiconductor in fabricating the OTFT. The thickness variation of the PVP layer was considered to optimize the device fabrication condition. The dielectric properties were estimated in terms of capacitance, dielectric strength and leakage current. The optimize device condition was PVP(45 nm)/YOx(100 nm) and PVP(70 nm)/YOx(100 nm) respectively. The successful deposition of the semiconductor layer on the surface of the dielectric depends on the surface nature of the dielectric. A smooth dielectric surface will facilitate homogeneous deposition of the semiconductor layer leading to less trap and more device performance. The PVP dielectric is generally considered superior over the PMMA dielectric layer as the former allows the deposition of the semiconductor layer via a solution processing. Later, Cao and his co-workers designed a solution-processed P3HT device using a double layer dielectric composed of anodized Ta2O5 (120 nm) and crosslinked PVP (250 nm). Tis device could result in an enhanced capacitance of 11.6 nFcm-2. The corresponding single layer device provided only 5.16 nF cm-2 [16]. In the year 2007, D. K. Hwang et al reported on the fabrication and characterization of pentacene based thin-film transistors with low-k poly-4-vinyl phenol(PVP)/high-k yttrium oxide (YOx)bilayer gate dielectrics of various thickness combinations, for the thin-PVP layers 45,70, and 140 nm and for the thin YOx 50 and 100 nm. Neither YOx nor thin-PVP single layer film alone can adequately function as a dielectric layer due to their very high leakage current. However, our bilayer films of six different thickness combinations among which the thinnest was PVP/YOx = 45/50 nm while the thickest was PVP/YOx = 140/100 nm all exhibited quite an excellent dielectric strength of ~2 MV/cm, based on our maximum leakage current standard of 10−6 A/cm2. All pentacene TFTs with the PVP/YOx bilayer gate dielectric films successfully demonstrated excellent TFT characteristics at an operating voltage less than -5 V [17]

Polymers that can be deposited by spin-coating, dip-coating, or inkjet-printing present a second major class of materials for the gate dielectric since most organic polymers are insulators by nature. It has been reported that several polymers show excellent insulating characteristics with very low leakage currents. Representative polymers are polystyrene (PS), polymethyl methacrylate (PMMA), poly(vinyl alcohol) (PVA), poly(vinyl phenol) (PVP), benzocyclobutene (BCB), parylene C and cyanoethyl pullulan (CYEPL). Their chemical structures are shown in Figure 1.



Fig.1: Chemical structure of (a) polystyrene (PS), (b) poly(methyl methacrylate) (PMMA), (c) poly(vinyl phenol) (PVP), (d) poly(vinyl alcohol) (PVA), (e) benzocyclobutene (BCB) and (f) parylene.

Common materials such as PS and PMMA were the first polymers to be used as gate dielectrics. However, PVA and PVP are two of the most widely used polymer dielectric materials. These can be deposited onto organic semiconductors because the solvents (aqueous for PVA and ethanol for PVP) for these materials are orthogonal to those used for the semiconductor.

The common polymers used for insulating purposes require a thick film (>300 nm) to achieve pinhole-free coatings with low gate leakage current. The resultant films provide low gate capacitance and, therefore, high operating voltages once TFT devices are constructed on them. The most popular way to reduce the thickness of polymer dielectric films while minimizing pinholes and retaining low leakage current is by cross-linking the polymer chains in the film during or after the polymer deposition. In this chapter, we have fabricated bottom-gate top contact pentacene based organic thin-film transistors (OTFTs) with organic-organic bilayer gate dielectrics and their electrical and surface parameters were evaluated. In our study, three different dielectrics were selected, cross-linked poly (vinyl phenol) (cPVP), cross-linked polyvinyl alcohol (cPVA) and poly(methyl methacrylate) (PMMA), because these three offer high field-effect mobility [18]. Despite its merits, PVP and PVA gate insulator has a fundamental drawback of degradation after fabrication of OTFTs due to their susceptibility to absorb moisture [19]. Here, we have cross-linked PVA and PVP to arrest the hydroxyl groups on their surfaces, and the resultant cPVP and cPVA have better immunity against moisture than PVP and PVA [20]. The motivation of this study is to compare the device performance of these bilayer dielectrics as compared to their single dielectric systems and to find the best bilayer dielectric combination in regards to low leakage current, smooth dielectric/OSC interface, high mobility and low threshold voltage.

**2. Synthesis of cPVP dielectric films based MIM and OTFT**

**2.1 Cross-linking in PVP and PVA:**

Poly-vinyl phenol and poly-vinyl alcohol have hydrophilic groups and thus can absorb moisture. Inorder to improve the dielectric performance it is necessary to make the surface of both he polymers hydrophobic before fabrication. Accordingly, cross-linking strategy has been used to form cross-linked PVP and PVA respectively.

PVP is dissolved in propylene glycol monomethylether acetate (PGMEA). Poly(melamine-co-formaldehyde) methylated (PMF) was added to the dissolved PVP in PGMEA to enable the crosslinking of the polymer molecules (figure 2). PVP crosslinking is a simple way to achieve a mechanically and chemically robust polymer film forming a “Bakelite” structure [19]. The solution is stirred for 1 hour at 60˚ then spin-coated at 3000 RPM for the 40s.

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Figure 2: Schematic representation of cross-linking of PVP

The PVA was cross-linked with ammonium dichromate (ADC) under UV irradiation [21] as shown in figure 3.

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Fig.3 Schematic representation of cross-linked polyvinyl alcohol

**2.2 Extraction of electrical parameters of OTFT:**

The electrical performance of OTFT is characterized by the parameters like field effect mobility (μ), threshold voltage (VT), on/off ratio and sub threshold swing (SS) using e following equations

**2.2.1 Field-effect-mobility and the threshold voltage:**

There are two working regions in an OTFT, i.e., linear region and the saturation region. In the linear region, the I-V can be expressed as –

$$ I\_{DS} =\frac{W}{L}μC\_{i}\left(V\_{G}-V\_{T}\right)V\_{DS } (1)$$

In the linear regime, the carrier field-effect mobility can be extracted from the transconductance gm, given as

$=-\frac{WμC\_{i}}{L}V\_{DS}$

Therefore, mobility for the linear region was given by-

$$μ=-g\_{m}\frac{1}{WC\_{i}V\_{DS}} (2)$$

The VT in the linear region can be obtained by fitting the transfer curve to a linear curve and the intercept to the horizontal axis.

In the saturation region, the I-V can be expressed as –

$$ I\_{DS}=\frac{W}{2L}μC\_{i}\left(V\_{G}-V\_{T}\right)^{2} (3)$$

Therefore, if we plot $\sqrt{I\_{DS}}$ as a function of VG, μ can be calculated from the slope of the transfer curve (k). As a result, μ can be calculated by the equation below-

$μ=\frac{2L}{WC\_{i}}K^{2}$ (4)

In the saturation region, VT can be obtained by the extrapolation of $\sqrt{I\_{DS}}$ versus VG curve to the horizontal axis.

**2.2.2 Current on-off ratio:**

It is an important parameter that characterizes the ability of an OTFT to switch a signal from off state to on state. A large current on-off ratio is desirable for a better performing OTFT. It depends on various factors such as the field effect mobility, thickness of the dielectrics and the semiconductor layers, channel length, etc. It is reported that devices with a short channel length results in high current on-off ratio. The current on-off is calculated from the following equation The formula for extraction of Ion/Ioff is calculated from equations (5) and equation (6)

(5)

(6)

Where Ci represents the insulator capacitance per unit area, µ is the mobility, VG is the gate voltage, VT stands for the threshold voltage, σ represents the channel conductivity, d is the semiconductor thickness and VD denoting the drain voltage respectively [22-23].

**2.2.3 Threshold voltage:**

The interface between the dielectric and the semiconductor plays an important role in OTFT. The information of the surface states and traps can be obtained from the threshold voltage (VT) in OTFT. It is reported in the literature that a thick pentacene layer and a shorter channel length can produce a low threshold voltage. A low value of VT allows to operate the device at a low voltage which is a desired property of commercial OTFTs [24]. The threshold voltage can be estimated by extrapolating the measured ID (or √ID) in the linear (or saturation) transfer characteristics to the intersection with the x-axis.

**2.2.4 Sub-threshold slope:**

Sub-threshold slope is defined as the measure of how fast the transition between the off- and on-states takes place. The sub-threshold is denoted by the region for gate-source voltages below the threshold voltage (VT) and above the turn-on voltage (VON). The turn-on voltage is the voltage on which the off-state current starts to increase dramatically. The Subthreshold slope (S) can be defined as the rate at which drain current varies (in decades) with gate voltage for device operated in the sub-threshold region. The turn-on characteristics of the OTFT devices can be described as by the following equation:

 (7)

S can be extracted by fitting a straight line to the steepest part in the sub-threshold region and then by calculating its inverse.

**2.2.5 Device fabrication:**

Various layers of the OTFT devices are deposited by vacuum evaporation and spin coating technique. For the dielectric characterisation, metal-insulator-metal (MIM) structures of Al/cPVP/Au with 100 nm, 120 nm and 140 nm thickness of cPVP respectively were fabricated first. Similarly, MIM structures of Al/cPVA/Au with 150 nm, 160 nm and 175 nm thickness of cPVA and Al/PMMA/Au with 170 nm, 200 nm and 220 nm thickness of PMMA respectively were fabricated. From the MIM structures, we have measured their current density versus electric field (J–E*)* and capacitance versus voltage (C-V) characteristics. These dielectric films were prepared with constant rotational speed of 3000 rpm for 40s and then annealed at 100 °C for 1 h on a hot plate in air. For the electrical characterisation, we have fabricated three sets of OTFT devices with varied thicknesses as applied in MIM devices described above. The device fabrication started with the deposition of patterned Aluminium (Al) with a thickness of 100 nm as a gate electrode on the glass substrate. For the first set of OTFT, the dielectric layer PVP cross-linked with Propylene Glycol Monomethyl Ether Acetate (PGMEA) was spin coated on the top of Al layer. We have varied the thickness of all dielectric layers for effective results shown in table 4.1. A layer of Pentacene of 50 nm thickness was thermally deposited over the gate dielectric layer at a rate of 0.6-0.8 Ǻ/s and a substrate temperature of 70 0C under high vacuum of 2x10-6 kPa by fixing the source to the substrate distance at 20 cm and for the oxides the distance is kept at 16 cm. The substrate temperature was kept at 70 0C during deposition because at that temperature best poly-crystalline thin films of pentacene can be grown. Finally, 80 nm thick gold (Au), used as a source/drain electrode, was thermally deposited on top of pentacene at a rate of 0.5 Ǻs-1 with a shadow mask of defined channel length (L) and channel width (W) of 50 µm and 1000 µm, respectively. All the layer thicknesses were measured using thickness profilometer. The prepared OTFT structures were annealed in vacuum at 1000C for 5 h. For the second set of OTFTs, the dielectric layer PVA cross-linked with ammonium dichromate was spin-coated over the Al layer at a rate 3000 rpm for the 30s. Similarly, for the third set of OTFTs, the dielectric layer PMMA diluted in toulene (5%) was used. The PMMA solution was spin-coated at 4000 rpm for 40s to form a uniform coating. Finally the film was baked at 170oC for 30 min in a conventional oven.

The structures of all the bottom gate OTFT devices used in this study are shown in figure 4(a-b).



Fig.4 Schematic diagram of (a) MIM structure and (b) OTFT where the dielectric layer consists of cPVP, cPVA and PMMA, respectively.

**2.2.6 Characterization of the dielectric films**

An important concern with gate dielectric materials is the gate leakage current. Figure 5 shows the leakage current for the capacitor with dielectrics cPVP as a function of the electric field applied. The capacitance-voltage (C–V) on an MIM structure was measured by an HP 4284 LCR meter at 10 kHz. From Fig. 5 it is seen that the capacitance of the cPVP dielectric film with 140nm thickness was found to be 22.4 nF/cm2, The dielectric constants of the bilayers were calculated by equation 8. The dielectric constant was estimated to be 3.6 for cPVP with 140 nm thickness value.



Fig.5 Plot of J-E characteristics measured with Al/cPVP/Au structure

The output and transfer curves of the fabricated OTFTs are presented fig.6(a-b). For the cPVP device, the characteristics show clear, well behaved linear (ohmic) regime and well saturated, relatively high ID in the regime.

Figure. 6 (a) output characteristics and (b) transfer characteristics of the cPVP dielectric OTFT with 140 nm thickness of cPVP

To obtain the output and transfer curves, figure 6(a-b), VD and VG for the devices with cross-linked PVP are varied at 0 to -10 V. The basic working principle of OTFTs is that the current between source and drain contacts (ID) in saturation is modulated by the gate bias (VG) according to equation 3. For V*D* more negative than V*G*, I*D* tends to saturate (saturation regime) owing to the pinch-off of the accumulation layer. The drain current for the cPVP dielectric film with 140 nm thickness was found to be only -50.2 μA. This indicates that the single layer dielectrics could not produce significantly higher drive current. The drain current was estimated at a drain voltage (VD) from 0-10V. Mobility of the device is calculated in the saturation regime using the *IDS* expression in equation 3. The devices with 140 nm cPVP layer shows mobility of 0.04 cm2/Vs. Figure 6b presents the graphical representation of (*ID*)1/2 vs *VG*. The threshold voltage (VT) is one of the important electrical parameter for determining the performance of organic thin film transistors. The threshold voltage relates to the electron density or charge density which are trapped in the region between the channel and OTFT’s contact places. This clearly indicates that the the threshold voltage is largely affected by the dielectric-OSC interface. Practically, VT is calculated from the linear part of the (*ID*)1/2 vs *VG*. The extrapolation of this linear portion to the *VG*.-axis is the *VT*. The surface roughness of the dielectric surface effect the OSC-dielectric interface as the rough surface creates more traps on the surface, which could be reason for high VT [25]. In our study, the threshold voltage is found to be -0.5V for the cross-linked PVP. One of the important electrical parameter which determines the improved performance of an organic thin film transistor is the current on-off (Ion-off) ratio. In our study, Ion-off ratio is estimated by using equation 6 and it was recorded as 1.7x102 for the cross-linked PVP dielectric. This can be correlated to the morphological analysis of pentacene over the dielectric (figure 7).The pentacene surface over the dielectrics was found to be smooth. The sub-threshold slope (S) is obtained by fitting a straight line to the steepest part in the sub-threshold region and calculating its reciprocal.

The surface topography of the pentacene films on the dielectrics was studied with atomic force microscopic (AFM) and x- ray diffraction (XRD) techniques. The surface roughness of the gate dielectric controls the growth of the deposited organic semiconductor film and thereby influences the device performance. The Atomic force microscopic (AFM) images of the pentacene growth over the dielectric is shown in fig 7. The RMS roughness values were calculated.

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 Fig. 7: AFM image of pentacene TFT with cPVP gate dielectrics.

Fig. 8: XRD spectra of Pentacene TFT with cPVP as the gate dielectrics.

The XRD spectra of the Pentacene TFT with cPVP is shown in figure 8. The XRD spectra of pure pentacene presents a sharp and highly intense peak at 5.70 which is also found in our study. Thus, this peak as shown in figure 8 is an evidence of the crystalline nature of pentacene growth over the cPVP dielectric surface.

**2.3 Pentacene-based organic thin-film transistors (OTFTs) using cPVP/cPVA as the bilayer gate dielectric.**

**2.3.1 Device fabrication:**

In our experiment, we have deposited the various layers of the OTFT devices by vacuum evaporation and spin coating technique. First of all, for the measurement of the capacitance and leakage current density, metal-insulator–insulator (MIM) devices were prepared by deposition of pentacene on the gate insulator-coated glass substrate. For the dielectric characterisation, we have first fabricated MIM structure of Al/cPVP/cPVA/Au with cPVP of 140nm thickness and cPVA thickness of 20, 30 and 50nm respectively and measured their J-E and C-V characteristics. After deposition of the Aluminium as the gate layer, a thin layer of PVP crosslinked with Propylene Glycol Monomethyl Ether Acetate (PGMEA), was spin-coated on Al layer at 3000 rpm for 40s as the first dielectric layer with a fixed thickness of 140 nm. The dielectric layer was then subjected to baking at150oC for 2 hrs. This was done in presence of oxygen and dry atmosphere. Similarly the deposition of the second dielectric layer was done. Cross-linked poly-vinyl alcohol was considered as the polymer for deposition of the second dielectric layer. This second layer was deposited using a spin coating machine keeping the rpm at 4000 with spinning time for 30 second. The second layer was deposited at three different thickness values at 20, 30 and 50 nm respectively. Finaly, these layers were subjected to baking at 170oC for 2 hrs in an oxygen atmosphere and dry air. Above the bilayer insulator layer, we have deposited the organic semiconductor layer of our devices using Pentacene through the evaporation mask maintaining a substrate temperature of 70o C. Finally, the Gold (Au) used as the source-drain layer of our devices has been fabricated using the evaporation mask of s-d through the specific channel length (L) and width (W). For investigating the effect of bilayer dielectric properly we have varied the thickness of the second dielectric layer at two stages.



Fig 9. Schematic diagram of (a) MIM structure and (b) OTFT device using cPVP/cPVA bilayer dielectric.

**2.3.2 Electrical properties of the cPVP based OTFTs**

The study of the electrical behavior of the metal insulator metal (MIM) devices provides useful information on the overall performance of the organic thin film transistors (OTFTs). Accordingly, we designed MIM capacitor on the glass substrate using cPVP/cPVA bilayer dielectric with a thickness variation of the cPVA layer at 20, 30 and 50 nm thicknesses respectively. The MIM devices were studied based on the current density vs electric field (J–E) graphical plots. Finally, pentacene, used as semiconductor, was deposited on the dielectric surface and its growth was monitored. The surface roughness of the dielectric layer greatly influence the dielectric-OSC interface [26-27]. Accordingly, the surface roughness values were recorded for the pentacene surface over the bilayer dielectric surface. Fig.10 (a-b) shows the J-E and C-V characteristics of the MIM structures of the Al/cPVP/cPVA/Pentacene with cPVA thickness of 20 nm, 30 nm and 50 nm respectively. Capacitance and leakage current density were measured on the MIM configuration. The bilayer dielectrics with 30 nm cPVA thickness exhibited low leakage current (<1x10-6A / cm2) as shown in J-E curve (Fig.10a). From the C-V measurements of the MIM structures, capacitance of the cPVP/cPVA bilayer dielectric films was measured. The obtained capacitance values were 30.7 nF/cm2, 37 nF/cm2 and 35.1 nF/cm2 with cPVA thickness 20nm, 30nm and 50nm respectively.

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Fig.10 Plots of (a) J-E and (b) C-V characteristics measured with Al/cPVP/cPVA/Pentacene structures with cPVP thicknesses of 20 nm, 30 nm and 50 nm respectively

From the MIM structure, the dielectric constants of the bilayers dielectrics are evaluated by using the equation 8.

$$C=\frac{k\in \_{o}A }{d} (8)$$

Where, k is the dielectric constant, A the area of the capacitor, d the dielectric thickness and 𝜀0 is the permittivity of free space

The output and transfer curves of the fabricated top-contact pentacene based OTFTs with cPVP/cPVA bilayer dielectrics with 20, 30 and 50 nm thick cPVA are presented in fig. 10(a-b) and 11. It has been observed that clear and ohmic regime with high drain current was obtained for all the three OTFT devices with the thickness values 20,30 and 50 nm respectively for the cPVA layer. The gate voltages were changed from 0V to -10 V in order to study the VD and VG behavior. On application of a negative bias on gate electrode, holes were accumulated in the dielectric-OSC interface. The accumulated holes form a conducting channel between the source and the drain and then move under the driving force of the source and finally enters in drain. For V*D* more negative than V*G*, I*D* tends to saturate (saturation regime) owing to the pinch-off of the accumulation layer [28]. Mobility of the devices are calculated in the saturation regime using the *IDS* expression in equation 3.

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Figure. 11 (a-c) Output characteristics and (d) transfer curves of the cPVP/cPVA bilayer dielectric OTFT with 20 nm, 30 nm and 50 nm thickness of cPVA respectively.

The largest current mobility was recorded at 0.53 cm2/Vsfor the OTFT device constructed with a dielectric thickness of 30 nm. Both the capacitance and the mobility of this device were found to be better as compared to the other two devices (figure 11d). The high capacitance value can be correlated with the increase in the mobility of the device. The high capacitance causes large number of charge carriers to be accumulated in the dielectric-organic semiconductor interface which eventually results in the increase in the mobility of the device [28].

The threshold voltage (VT) is one of the important electrical parameter for determining the performance of organic thin film transistors [29]. The threshold voltage relates to the electron density or charge density which are trapped in the region between the channel and OTFT’s contact places. This clearly indicates that the the threshold voltage is largely affected by the dielectric-OSC interface. Practically, VT is calculated from the linear part of the (*ID*)1/2 vs *VG*. The extrapolation of this linear portion to the *VG*.-axis is the *VT*. The surface roughness of the dielectric surface effect the OSC-dielectric interface as the rough surface creates more traps on the surface, which could be reason for high VT [30]. In our study, the threshold voltage is found to be -2.5V for the cPVP and cPVA dielectric layers (Table 1).

One of the important electrical parameter which determines the improved performance of an organic thin film transistor is the current on-off (Ion-off) ratio. In our study, Ion-off ratio is estimated by using equation 6 and it was recorded as 1.8×105 for the cPVP-cPVA dielectric with 30 nm thickness for the cPVA layer. This can be correlated to the morphological analysis of pentacene over the dielectric (figure 12). The improvement in the current on-off ratio can be correlated to the deposition of the second dielctric layer of 30 nm thickness which reduces the current leakage tendency (fig. 11a). The sub-threshold slope (S) is obtained by fitting a straight line to the steepest part in the sub-threshold region and calculating its reciprocal. The sub-threshold swing represents the speed of a transistor switches from the off state to the on state. The sub-threshold slope (S) is obtained by fitting a straight line to the steepest part in the sub-threshold region and calculating its reciprocal. The sub-threshold slope values are presented in table 1.

Table 1 Electrical and surface parameters of the fabricated OTFT devices with cPVP/cPVA as bilayer dielectrics.

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| cPVP/cPVA(nm) | RMS Surface roughness (nm)  | Mobility,µ(cm2/Vs) | Threshold voltage, VT(V) | Current on-off ratio, Ion-off | Sub-threshold slope,S (V/decade) |
| 140/20 | 0.749 | 0.31 | -2.00 | 2.8x104 | 0.78 |
| 140/30 | 0.751 | 0.53 | -2.50 | 1.8x105 | 0.36 |
| 140/50 | 0.762 | 0.29 | -2.80 | 4.1x104 | 0.89 |
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| **(a)** | **(b)** |

Figure 12: AFM image of pentacene growth over (a) cPVP and (b) cPVP/cPVA with 30nm thick cPVA as dielectrics

The Atomic force microscopic (AFM) images of the pentacene growth over the dielectrics are shown in fig. 12(a-b).The RMS roughness values were calculated and are presented in Table 1a. The OTFT with Al/cPVP(140)/cPVA(30nm)/Pentacene/Au, produced the lowest RMS value, which indicates uniform deposition of the pentacene layer over the dielectric surface. In other words it may also be concluded that the quality of the dielectric-OSC interface has improved with the thickness variation of the cPVA layer. As a result, the electrical parameters of the pentacene TFT with cPVA (30nm) as the gate dielectric has also improved in comparison to the other two devices (Table 1). The field emission scanning electron microscopic (FESEM) images of the prepared devices were taken to study the surface morphology (fig 13). The smooth surface of pentacene growth is observed in the SEM study. The observation in SEM complements the AFM observations.



Figure 13: FESEM image of pentacene grown over(a) cPVP and (b) cPVP/cPVA(30nm)

The XRD spectra of the Pentacene TFT with cPVP/cPVA with 30 nm thick cPVA layer is shown in figure 14.



Figure 14: XRD spectra of pentacene grown over cPVP/cPVA(30nm) dielectric.

The characteristic peak of pentacene at 5.70 is observed. The crystalline growth of pentacene over the dielectric surface is also observed in the FESEM and AFM studies. Comparing the results obtained for each of the devices, it was found that our fabricated pentacene TFT with cPVA with 30nm as the gate dielectric exhibited better OTFT parameters. To enhance the electrical parameters, the dielectric surfaces are to be made smooth and defect free with low values of RMS surface roughness and with crystalline growth of the semiconductor over the dielectric surfaces.

**4. Conclusion**

The importance of bilayer gate dielectric films in the development of organic thin film transistors are wll presented. The Pentacene TFT devices with cPVP/cPVA as the gate dielectric was studied in a bottom gate top contact configuration using aluminium (Al) as gate and gold (Au) as the source/drain electrode respectively. Among all the bilayer devices Al/cPVP/cPVA(30nm)/Pentacene/Au exhibited the best electrical parameters. The carrier mobility, on-off current ratio, sub-threshold swing and threshold voltage are 0.53 cm2/Vs, 1.8x105, 0.36 and -2.5 V respectively. The surface and crystalline growth of pentacene with large grain sizes over the cPVA layer is largely responsible for the better electrical performance in comparison of cPVP/cPVA devices of this chapter.

**5. Future recommendations**

The demand of novel and flexible dielectrics in electronics is growing day by day. Detailed review on past and present methods of synthesis, characterization techniques alongwith commercial applications is the need of the hour. The presented cPVP and cPVP/cPVA gate dielectrics are needed to be tailored further to find commercial applications. Ultraflexible dielectric materials with high current mobility is the future trend in dielectric materials in electronics applications.

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