Design and Performance Analysis of Ternary D Latch Applying Carbon Nano Tube Field Effect Transistor

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Abstract-**Carbon Nanotube Field Effect Transistors (CNTFET) have been extensively investigated after the silicon MOSFETs now a day. In case of CNTFET, the threshold voltage can be altered by regulating the chirality vector which is the diameter of CNT. As CNTFET is an encouraging substitute for the Multiple-Valued Logic (MVL) design, this technique employing the ternary is feasible for high performance as well as low-power VLSI designs. In this work, a compact structure of MOSFET called CNTFET has been developed. The analysis of the CNTFET is carried out initially. The I-V characteristics based on chirality is analysed, and a novel design of ternary D latch applying CNTFETs is suggested and compared with prevailing D latch designs.**

Index Terms—Multiple-Valued Logic (**MVL)**, **CNTFET**, Standard Ternary Inverter (**STI)**, Positive Ternary Inverter (**PTI**), Negative Ternary Inverter (**NTI).**

I. INTRODUCTION

Ternary logic is a favorable substitute for the basic binary logic design system. It promises to achieve clarity as well as energy optimization in digital electronics by reason of the minimized circuitry of interconnects and chip area. Usually, digital calculations are executed on a two-valued logic functions, i.e., binary '0' and '1'. Multiple-valued logics (MVL) substitutes the conventional Boolean definition of variables with either finitely or infinitely different values like ternary logic [1] or fuzzy logic [2]. Ternary logic or three-valued logic, being one of those, has attracted important notice for its latent gains over simple binary logic. The ternary logic gates can be used to implement decoding digital designs because of the requirement of fewer gates, whereas binary logic can be used to implement fast computing logic.

In recent years, the MOSFET has been utilized as a fundamental device for designing of a circuit [3]. While the minimization in size of silicon-based circuits approaches its physical constraints, researchers are working to implement new material and techniques that preserves the characteristics of the existing silicon technology as well as to overcome the problem related with physical size limitations. The CNTFET is a favorable replacement to the large silicon transistor with low-power consumption and high-performance characteristics. The CNTFET based devices exhibits high carrier velocity for fast switching as well as high mobility for near-ballistic transport. HSPICE adaptable CNT structure is applied to design binary circuits, and simulation is performed on Avanwaves. In this article, the Carbon nanotubes is introduced in section II. Section III and IV reviews Ternary Logic. In section V and VI simulation outcomes and parameter evaluation of digital circuits are shown.

II. THE CARBON NANOTUBE FET

Carbon Nanotube FET are hollow cylinders with diameters varying from 1nm to 50nm and lengths over 10μm [4]. The carbon atoms are fixed into hexagons which form a honeycomb arrangement. A nanotube can be observed as a single layer or multilayer of graphite coiled into a smooth cylinder, as depicted in Fig.1. Two categories of nanotubes are available; one is the single-wall nanotube (SWCNT) which is build up of a single layer of graphite or graphene sheet, and second one is a multiwall nanotube (MWCNT) which has multiple shells [5].

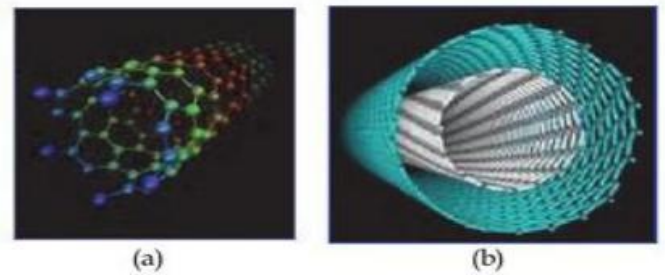

Fig.1. Physical model of Nanotubes, (a) SWCNT (b) MWCNT

Fig.2. Schematic figure of a CNTFET

The graphene is folded by a pair of integers (n, m) named as chiral vectors. With the help of the chiral vector of a CNT, one can find out whether the CNT is metallic or semiconducting type. The nanotube is metallic if n=m or n-m=3i, where i is an integer. Alternatively, the tube is semiconducting. The diameter of the CNT may be calculated using the following expression [6][7].

$$D_{CNT}=\frac{\sqrt{3}a_0}{\pi}\sqrt{m^2+n^2+mn} \quad (1)$$

Whereby a_0=0.144 nm is the inter-atomic distance between each carbon atom and its neighbor. Figure 3 shows the schematic diagram of CNTFET.

The current vs. voltage (I-V) plots of the CNTFET are identical to MOSFETs with higher performance. The threshold voltage is represented as the voltage needed to switch on a transistor. The threshold voltage of the intrinsic CNT channel can be written as,

$$V_{th}=\frac{E_g}{2e}=\frac{\sqrt{3}aV_\pi}{3eD_{CNT}} \quad (2)$$

Whereas a=2.49 A^0 is the carbon to carbon atom distance, e is the unit electron charge, Vπ=3.033 eV is the carbon π-π bond energy in the tight bonding model, as well as D_{CNT} is the CNT diameter. For example, the threshold voltage of a CNTFET with chirality (13, 0) CNT is 0.428 V, compare to a CNTFET using (19, 0) CNT with the threshold voltage of 0.293 V [8][9]. The threshold voltages of CNTFETs that are used in this work are given in Table1. These values are evaluated applying the diameter of every CNTFET and by utilizing the expression of (2). The threshold voltage of the CNTFET is inversely proportional to the chirality vector of the CNT which is depicted in Figure 3.

Diameter of CNTFET	Threshold Voltage of CNTFET
D=1.487 nm(19, 0)	0.293 V
D=1.018 nm(13,0)	0.428 V
D=0.783 nm(10,0)	0.557 V

Table I. Diameter of CNTFETs and the corresponding threshold voltages

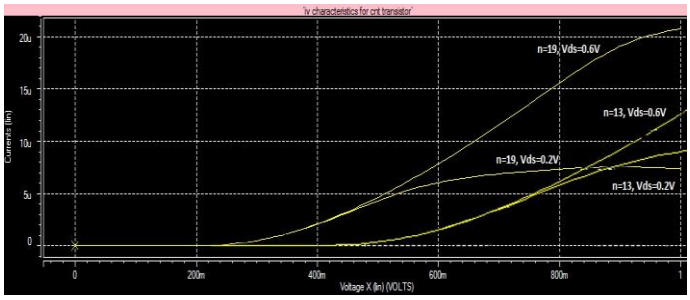

Fig.3.Id Vs. Vgs plot for n-CNTFET

III. TERNARY LOGIC CONCEPT

Ternary logic has three meaningful values in comparison with binary logic that has two values. These values are written as false, undefined, and true, respectively and are denoted as 0, 1, and 2. Any n variable (x1,…, xn) ternary function f(X) is represented as a function mapping $\{0,1,2\}^n$ to {0,1,2}, where X={$X1,\dots Xn$}. The fundamental working of ternary logic can be expressed as below, Whereby Xi, Xj= {0,1,2}, [10]

$$\text{Xi + Xj} = \max\{Xi, Xj\}$$

$$\text{Xi*Xj} = \min\{Xi, Xj\} \quad (3)$$

$$\bar{\text{X}}\text{i} = 2 - \text{Xi}$$

Whereby '-' indicates the mathematical subtraction and the operators *, +, and bar refer to AND, OR, and NOT in ternary logic, respectively. The ternary logic levels and values are given in Table II.

Voltage Level	Logic Value
0	0
1/2Vdd	1
Vdd	2

Table II: Logic Values

A. Ternary Inverter

Ternary Inverter is a basic gate in the ternary logic method. A conventional ternary inverter is denoted as an operator with one input x as well as three outputs y_0, y_1, and y_2.

$$y_0 = \text{C0(x)} = \begin{cases} 2, & x = 0 \\ 0, & x \neq 0 \end{cases}$$

$$y_1 = \text{C1(x)} = \begin{cases} 2, & x \neq 2 \\ 0, & x = 2 \end{cases} \quad (2)$$

$$y_2 = \text{C2(x)} = \bar{X}i = 2 - \text{Xi}$$

Hence, the operation of a ternary inverter would require three inverters. They are a Negative Ternary Inverter (NTI), a Positive ternary inverter (PTI), a Standard Ternary Inverter (STI). The truth table of the three ternary inverters is given in Table III.

Input X	PTI	NTI	STI
0	2	2	2
1	2	0	1
2	0	0	0

Table III: Truth table of PTI, NTI, and STI

B. Ternary NOR as well as NAND gates

The Ternary NOR and NAND gates are multiple input gates applied in the Ternary Logic system. For the two inputs X1

and X2, the function for the Ternary NOR and NAND gates are expressed by the below equations.

$$Y_{nand}=\overline{\min\{X_I, X_J\}}$$

$$Y_{nor}=\overline{\max\{X_I, X_J\}}$$

Input X2	Input X1	Y_{nand}	Y_{nor}
0	0	2	0
0	1	2	0
0	2	2	0
1	0	2	0
1	1	1	1
1	2	1	1
2	0	2	2
2	1	1	1
2	2	0	0

Table IV: Truth table of Ternary NAND as well as NOR gates

IV. TERNARY D-LATCH DESIGN SUBJECT TO CNTFET

D-latch is extensively utilized as a storage device. This memory device retains precisely one of the logic levels unless the control inputs or enables change. Depending on this principle, a novel D-latch design is initiated using 1-p type CNTFET, 2-n type CNTFET, 2-STI, and 1-NTI. For STI, NTI and PTI, the design is shown in figure 4. The operation of the latch is given below. When Enable is logic '0', then the output at Q is the identical as the input data (Din). When Enable is logic '2', then the output at Q is identical as previous data at Q.

EN	DIN	Q	$\bar{Q}$
0	0	0	2
0	1	1	1
0	2	2	0
2	X	$Q_{prev.}$	$\overline{Q_{prev.}}$

Table V: Operational table for proposed D Latch

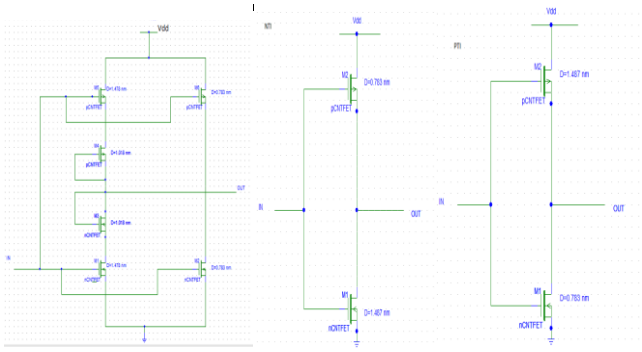

Fig.4. Proposed STI, NTI, and PTI

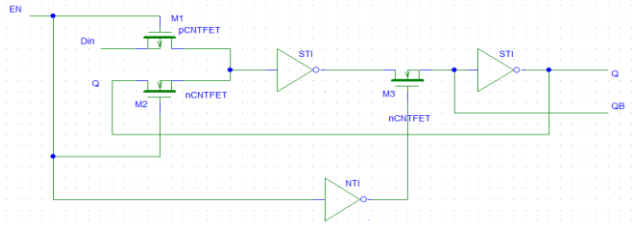

Fig.5. Proposed Ternary D-Latch applying basic gates

V. SIMULATION RESULTS

H-Spice Simulation is used to simulate the proposed design and are shown in fig 5, 6. Results show that the logic resource utilization, power and delay more efficient than earlier techniques [10].

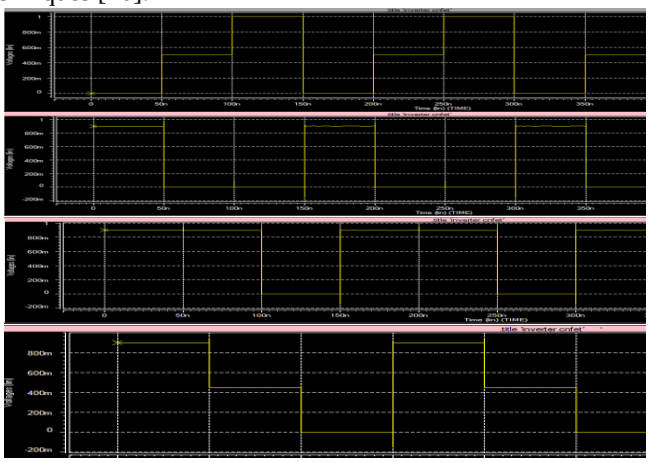

Fig.6. Simulation result for NTI, PTI, and STI

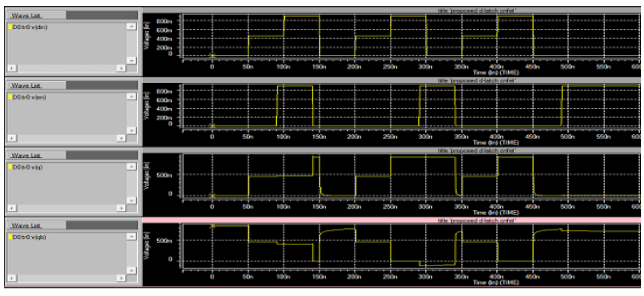

Fig.7. The transient response of proposed D latch

VI. RESULT AND DISCUSSION

The power supply voltage of 0.9 V as the default value of the CNTFET model [8] is applied. Logic 0 corresponds to a voltage less than 0.3 V, logic 1 corresponds to a voltage value between 0.3 V and 0.6 V, and logic 2 corresponds to a voltage value greater than 0.6 V.

In the average power dissipation, the CMOS-based design consumes a higher amount of power next to conventional CNTFET based design, followed by CNTFET design using ternary logic gates.

To compare the proposed and existing design, delay, PDP (power-delay product) and power dissipation of three designs are evaluated. We calculated PDP as a product of power and delay, Table VI, due to trade-off between the power consumption and delay.

The PDP is an important parameter, and simulated by HSPICE. It has been shown in fig.4, Fig.5 that the proposed design has less power and delay compared to the existing design. The PDP of the existing design is higher than the proposed design. Since transistor count is the most crucial property, thus we proposed a new design.

As the CNTFET threshold voltage depends on the diameter of nanotubes, by changing the CNTFET chirality, circuits can be designed..

Fig.7 shows the simulation results of the proposed design using HSPICE. It shows that proposed ternary D-latch is working based on the CNTFET model given in [11].

The ternary information present at input (Din) of D latch is carried out to Q output while enabling (En) input is low '0'. When enable is high '2', the ternary information at the data input at the time the transition occurred is retained at Q output until the enable input is low '0' again.

Parameters	Binary	Existing Ternary D-latch	Proposed
Power(watts)	3.0046E-06	9.1109E-07	7.1305E-07
Delay	7.5042E-11	-2.4474E-08	-9.9347E-07
PDP	22.5471E-17	-22.2933E-15	-70.8393E-14

Table VI: Comparison of power, delay, and PDP

VII. CONCLUSION

The D-latch design for ternary logic has implemented using the CNTFET technology. Since the threshold voltage level of the CNTFET is a function of the geometry of the CNTFET, an innovative multi-diameter CNTFET based ternary logic design is analysed. As CNTFET is an encouraging substitute for the MVL logic design, this design technique employing the ternary is feasible for high performance and low-power VLSI designs. It has the advantages of reduction in the circuit complexity, low power consumption, and high speed.

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