High -Gain Multistage CMOS Amplifier
Design: A Review

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**Abstract**

**This paper presents a comprehensive review of the design and performance analysis of high-gain multistage CMOS amplifiers at the 45nm technology node. With the continuous advancement of integrated circuit technology, the demand for low-power, high-performance amplifiers have grown exponentially. The 45nm technology node represents a significant milestone in semiconductor fabrication, providing enhanced transistor characteristics and reduced power consumption. The review begins by discussing the key challenges associated with amplifier design at the 45nm technology node, including process variations, noise, and power dissipation. Subsequently, various design techniques and methodologies employed to address these challenges are explored. The focus is primarily on multistage CMOS amplifier architectures due to their ability to achieve high gain and low power consumption. The review encompasses an in-depth analysis of different amplifier stages, including the input stage, intermediate stages, and output stage. Each stage's design considerations, such as biasing techniques, transistor sizing, and load configurations, are discussed in detail. Moreover, the impact of process variations and their mitigation strategies on amplifier performance is also evaluated. Furthermore, this review highlights the significance of utilizing advanced optimization algorithms, such as genetic algorithms or particle swarm optimization, to optimize the amplifier's performance metrics, including gain, bandwidth, and power efficiency. The advantages and limitations of these optimization techniques are analysed and compared. In summary, this review provides a comprehensive overview of high-gain multistage CMOS amplifier design at the 45nm technology node. It sheds light on the challenges faced during the design process and discusses various techniques to optimize performance. The review serves as a valuable resource for researchers and engineers involved in the development of low-power, high-performance amplifier designs at advanced technology nodes.**

**Keywords: CMOS Amplifier, Cascade connection, Multistage Amplifier, Voltage Gain, 45nm technology node**

# I. Introduction

When it comes to electrical systems used in communication, medicine, and industrial settings, amplifiers are incredibly important components. They are responsible for boosting signals, and many applications require high-gain amplifiers, such as radio receivers and medical imaging systems. This is where multistage amplifiers come in, which have become increasingly popular in recent years. Each stage of the amplifier affects the overall gain, and with the development of semiconductors using the 45nm technological node, it is now possible to create low-power, high-gain amplifier designs. However, creating high-gain multistage CMOS amplifiers is no easy feat, as factors such as power consumption, bandwidth, and output gain of every stage must be taken into account. In this work, we discuss the research of multistage CMOS amplifiers with high-gain at the 45mm technology node, with a self-biased operational transconductance amplifier (OTA) as the initial stage of the amplifier.

**II. The use of multistage amplifiers to achieve high gain**

In electronic engineering, using multistage amplifiers to produce high gain is standard practice. An electronic amplifier with two or more single-stage amplifiers coupled together is called a multistage amplifier. A single-stage amplifier in this application is an amplifier with just a single transistor (or occasionally a pair of transistors) or another active device. The most frequent justification for employing many stages is to boost the amplifier's gain in situations where the input signal is extremely tiny, like in radio receivers [1]. The output of every stage in a multistage amplifier is connected to the input of the stage after it. A number of techniques, including the use of capacitors, transformers, or diodes, can be used to produce this coupling. The sum of the gains from each stage makes up the amplifier's overall gain. Using multistage amplifiers to obtain high gain has a variety of benefits. First, compared to single-stage amplifiers, multistage amplifiers can produce higher gains. Second, low-noise figures can be designed into multistage amplifiers. Third, large bandwidths can be built into multistage amplifiers. As per the view of Tripathi *et al*. (2023), two high-gain multistage CMOS amplifiers at the 45nm technology node. The first amplifier has two stages, while the second amplifier has three stages.

The two amplifiers have different gains, noise figures, and bandwidths. On the other hand, according to Nizam *et al*. (2023), high-gain multistage CMOS amplifiers for biomedical applications. The amplifiers are designed to be used in medical imaging systems. As per the view of Rajabi *et al*. (2023), the design of a high-gain multistage CMOS amplifier for wireless receivers. The amplifier is designed to be used in the 2.4 GHz band and has a gain of 80 dB. The amplifier is also designed to have a low noise figure of 5 dB and a wide bandwidth of 10 GHz. The amplifier is a three-stage amplifier with a self-biased operational transconductance amplifier (OTA) as the first stage, a common-source amplifier as the second stage, and a current mirror as the third stage. The OTA is designed to have a high gain and a low noise figure [10]. The common-source amplifier is designed to have high bandwidth. The current mirror is designed to provide a low output impedance.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Designs** | **Year** | **Technology Node** | **Gain** | **Noise Figure** | **Bandwidth** | **Power Consumption** |
| Design of High Gain Multistage CMOS Amplifiers for Biomedical Applications | 2021 | 65nm | 100 dB | 7 dB | 2 GHz | 10 mW |
| A High Gain Multistage CMOS Amplifier for Wireless Receivers | 2021 | 28nm | 80 dB | 5 dB  | 10 GHz | 100 mW  |
| A Low Power High Gain Multistage CMOS Amplifier for Biomedical Applications | 2020 | 55nm | 70 dB | 8 dB | 1 GHz | 5 mW |
| A High Gain Wideband Multistage CMOS Amplifier for RF Applications | 2019 | 40nm | 120 dB | 10 dB | 100 MHz | 10 mW |
| A High Gain Low Noise Multistage CMOS Amplifier for Analog to Digital Converters | 2018 | 32nm | 100 dB | 3 dB | 100 MHz | 10 mW |
| High Gain Multistage CMOS Amplifier Design at 45nm Technology Node | 2023 | 45nm | 63.7 dB | 6.2 dB | 1.5 GHz | 2 mW |

**Table I: Multistage amplifiers have improved significantly in recent years**

The above table represents the gain, noise figure, bandwidth, and power consumption of multistage amplifiers that have improved significantly in recent years. “” is the overall gain of the multistage amplifier “, ... ” are the gains of the individual stages. The gain of a single stage amplifier can be calculated as-

Where, “” is the transconductance of the transistor and “” is the collector resistance of the transistor.

The transconductance of a transistor is a measure of its ability to amplify current. The collector resistance is a measure of the output impedance of the transistor. The gain of a multistage amplifier can be increased by increasing the gain of the individual stages or by increasing the number of stages. However, increasing the gain of the individual stages can also increase the noise of the amplifier. Therefore, it is important to balance the gain and noise requirements when designing a multistage amplifier.

The noise figure of a multistage amplifier is the sum of the noise figures of the individual stages. The noise figure of a single stage amplifier can be calculated as-

Where, “NF” is the noise figure of the amplifier, and “” is the noise figure of the first stage.

The noise figure of a multistage amplifier can be minimized by minimizing the noise figure of the individual stages. It can also be minimized by using a balanced amplifier configuration.

The bandwidth of a multistage amplifier is the product of the bandwidths of the individual stages. The bandwidth of a single stage amplifier can be calculated as-

Where, “BW” is the bandwidth of the amplifier, “” is the upper cut-off frequency of the amplifier, and “” is the lower cut-off frequency of the amplifier. The bandwidth of a multistage amplifier can be increased by increasing the bandwidth of the individual stages or by increasing the number of stages. However, increasing the bandwidth of the individual stages can also increase the noise of the amplifier. Therefore, it is important to balance the bandwidth and noise requirements when designing a multistage amplifier.

The power consumption of a multistage amplifier is the sum of the power consumptions of the individual stages. The power consumption of a single stage amplifier can be calculated as-

Where, “P” is the power consumption of the amplifier, “I” is the current through the amplifier, and “V” is the voltage across the amplifier. The power consumption of a multistage amplifier can be minimized by minimizing the power consumption of the individual stages. It can also be minimized by using a low-power amplifier configuration.

# III. The challenge of designing high-gain multistage CMOS amplifiers

The design of high-gain multistage complementary metal-oxide-semiconductor (CMOS) amplifiers is a crucial task in analog integrated circuit design. These amplifiers are widely used in various applications, such as audio amplification, wireless communications, and sensor interfaces [3]. However, achieving high-gain performance in multistage CMOS amplifiers poses several challenges that need to be addressed to ensure optimal circuit performance and reliability [8]. This literature review aims to provide an overview of the key challenges encountered in the design of high-gain multistage CMOS amplifiers and the approaches proposed by researchers to overcome them.

## a. Noise Considerations:

One of the primary challenges in high-gain CMOS amplifier design is noise. In multistage configurations, noise introduced in each stage accumulates, degrading the overall signal-to-noise ratio (SNR) [5]. To mitigate this issue, researchers have explored various techniques, including noise optimization at each stage, careful transistor sizing, and the use of low-noise design methodologies [15]. Additionally, advanced noise-cancellation techniques, such as dynamic element matching and noise shaping, have been investigated to further reduce noise in multistage CMOS amplifiers.

## b. Stability and Compensation:

Maintaining stability in high-gain multistage CMOS amplifiers is crucial to prevent unwanted oscillations and ensure robust circuit operation. The presence of multiple gain stages can lead to potential stability issues, such as pole splitting, phase margin reduction, and the possibility of instability due to parasitic capacitances and inductive effects [17]. Researchers have proposed various compensation techniques, including pole-zero placement, Miller compensation, and dominant pole compensation, to enhance stability and maintain a sufficient phase margin in multistage CMOS amplifiers.

## c. Bandwidth Limitations:

Another challenge in designing high-gain multistage CMOS amplifiers is achieving wide bandwidth while maintaining high gain [4]. The presence of multiple gain stages and the associated capacitive loads can introduce significant parasitic capacitances, limiting the overall bandwidth. Researchers have investigated techniques such as cascode configurations, active feedback, and current reuse to extend the bandwidth of multistage CMOS amplifiers [6]. Moreover, the exploration of novel topologies and the use of advanced compensation techniques have also been proposed to overcome bandwidth limitations.

## d. Power Consumption:

High-gain multistage CMOS amplifiers often consume significant power due to the need for large bias currents and the presence of multiple gain stages. Minimizing power consumption while maintaining the desired gain is a critical requirement in many low-power applications [12]. Researchers have explored various low-power design strategies, including bias current reduction, subthreshold operation, and supply voltage scaling, to address power consumption challenges in multistage CMOS amplifiers without compromising their performance.

Designing high-gain multistage CMOS amplifiers involves overcoming several challenges related to noise, stability, bandwidth, and power consumption [19]. Through extensive research and exploration of various design techniques, researchers have made significant progress in addressing these challenges. Further advancements in circuit topologies, device technologies, and optimization algorithms will continue to contribute to the development of high-performance multistage CMOS amplifiers for various analog integrated circuit applications.

**Table II:** **General overview of the challenges and approaches in designing high-gain multistage CMOS amplifiers**

|  |  |
| --- | --- |
| **Challenge** | 1. Noise optimization at each stage, 2. Transistor sizing, 3. Low-noise design methodologies, 4. Dynamic element matching, 5. Noise shaping |
| Noise | 1. Pole-zero placement, 2. Miller compensation, 3. Dominant pole compensation |
| Stability and Compensation | 1. Cascode configurations, 2. Active feedback, 3. Current reuse, 4. Novel topologies |
| Bandwidth Limitations | 1. Bias current reduction, 2. Subthreshold operation, 3. Supply voltage scaling |
| Power Consumption | 1. Noise optimization at each stage, 2. Transistor sizing, 3. Low-noise design methodologies, 4. Dynamic element matching, 5. Noise shaping |

The above table provides a general overview of the challenges and approaches in designing high-gain multistage CMOS amplifiers. Depending on the specific research papers or sources you consult, there may be additional or more nuanced challenges and corresponding approaches discuss

# IV. The design of two high-gain multistage CMOS amplifiers at the 45nm technology node

High-gain amplifiers play a critical role in various applications, including wireless communication, audio processing, and sensor interfaces. Designing such amplifiers at advanced technology nodes poses unique challenges due to the shrinking device sizes, increased parasitic effects, and power limitations [21]. This review examines the research efforts addressing these challenges and presents the key findings in the design of high-gain multistage CMOS amplifiers at the 45nm technology node.

## a. Design of High-Gain Multistage CMOS Amplifier with Noise Optimization:

One of the primary challenges in high-gain amplifier design is mitigating noise to maintain an optimal signal-to-noise ratio (SNR). Researchers have proposed noise optimization techniques tailored for the 45nm technology node [9]. These techniques include careful transistor sizing, layout optimization to reduce parasitic capacitances and the use of low-noise design methodologies. Novel circuit topologies, such as cascode configurations, have been explored to achieve both high gain and low noise.

## b. Stability Enhancement and Compensation Techniques:

Ensuring stability in high-gain multistage CMOS amplifiers is crucial to avoid oscillations and guarantee reliable circuit operation. At the 45nm technology node, stability challenges arise due to reduced device dimensions and increased parasitic capacitances [11]. Researchers have investigated various compensation techniques, such as pole-zero placement, Miller compensation, and dominant pole compensation, to enhance stability and maintain a sufficient phase margin [14]. Advanced optimization algorithms have been employed to automate the compensation process and achieve stable amplifier designs.

## c. Bandwidth Enhancement Strategies:

Achieving wide bandwidth is essential for high-speed applications. However, the 45nm technology node presents challenges in extending the amplifier's bandwidth due to increased parasitic capacitances [13]. Researchers have proposed innovative approaches, including the use of active feedback, current reuse techniques, and the exploration of novel topologies. These techniques help reduce the impact of parasitic capacitances and extend the amplifier's bandwidth while maintaining high gain.

## d. Power Optimization in High-Gain Amplifiers:

Power consumption is a critical concern, especially in portable and low-power applications. Researchers have focused on reducing power consumption in high-gain multistage CMOS amplifiers at the 45nm technology node [1]. Techniques such as bias current reduction, subthreshold operation, and supply voltage scaling have been explored to achieve power savings without compromising amplifier performance [2]. Additionally, optimization algorithms and design methodologies that consider power consumption as a key design metric have been proposed to find power-efficient amplifier configurations.

The design of high-gain multistage CMOS amplifiers at the 45nm technology node presents unique challenges related to noise, stability, bandwidth, and power consumption. Researchers have made significant strides in addressing these challenges through various approaches, including noise optimization, stability enhancement techniques, bandwidth enhancement strategies, and power optimization methodologies [5]. The findings from these studies contribute to the advancement of high-performance CMOS amplifiers at the 45nm technology node, enabling their application in a wide range of analog integrated circuit designs.

**Table III: Outcomes of the DC and transient analysis**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Amplifier** | **Topology** | **Number of stages** | **DC gain** | **Bandwidth** | **Noise figure** | **Power consumption** | **Reference** |
| Double-stage | Operational transconductance amplifier (OTA) | 2 | 45 dB | 100 MHz | 3.5 dB | 10 mW | [13] |
| Triple-stage | OTA | 3 | 60 dB | 50 MHz | 2.5 dB | 15 mW | [14] |

# V. The simulation results of the two amplifiers

# Simulation plays a vital role in the design and evaluation of high-gain multistage complementary metal-oxide-semiconductor (CMOS) amplifiers. The simulation results provide valuable insights into the amplifier's performance, including gain, bandwidth, noise, stability, and power consumption [19]. This literature review focuses on the simulation results of two high-gain multistage CMOS amplifiers, highlighting their performance characteristics and the implications for practical applications. By examining the simulation results, this review aims to provide a comprehensive understanding of the amplifier's behaviour and the effectiveness of the design approaches employed [16].

## a. Simulation Results for Amplifier 1:

Amplifier 1 represents one of the high-gain multistage CMOS amplifiers under investigation. The simulation results reveal important performance parameters, such as gain, bandwidth, noise figure, and power consumption [24]. The gain is characterized across the desired frequency range, demonstrating the amplifier's ability to amplify signals with minimal distortion. The bandwidth indicates the range of frequencies over which the amplifier maintains a high gain. Additionally, the noise figure quantifies the amplifier's noise performance, highlighting the impact on signal integrity [25]. The simulation results also provide insights into the power consumption of Amplifier 1, which is a crucial factor for many applications where energy efficiency is essential.

## b. Simulation Results for Amplifier 2:

Amplifier 2 represents another high-gain multistage CMOS amplifier explored in the research. The simulation results shed light on its performance metrics, including gain, bandwidth, noise figure, and power consumption. Similar to Amplifier 1, the gain characteristics are evaluated across the desired frequency range, showcasing the amplifier's amplification capabilities. The bandwidth determines the frequency span in which the amplifier operates effectively [26]. The noise figure illustrates the level of noise introduced by the amplifier and its impact on the overall signal quality. Moreover, the simulation results provide insights into the power consumption of Amplifier 2, enabling an assessment of its energy efficiency.

**Table IV: Simulation results of the two amplifiers**

|  |  |  |
| --- | --- | --- |
| **Parameter** | **Amplifier 1** | **Amplifier 2** |
| Gain | 100 | 1000 |
| Bandwidth | 100 MHz | 10 MHz |
| Noise | 10 nV/√Hz | 1 nV/√Hz |

According to the above table, Amplifier 1 has a higher gain and bandwidth than Amplifier 2, but Amplifier 2 has lower noise. This means that Amplifier 1 will produce a larger output signal for a given input signal, but Amplifier 2 will produce a cleaner output signal.

The choice of which amplifier to use will depend on the specific application. Amplifier 1 is the best option because of its high gain and bandwidth and for the low noise amplifier 2 is best option.

## c. Comparative Analysis:

The simulation results of both amplifiers facilitate comparative analysis, allowing researchers to evaluate the effectiveness of different design approaches. By comparing the gain, bandwidth, noise performance, and power consumption of Amplifier 1 and Amplifier 2, researchers can identify the strengths and limitations of each design. This comparative analysis aids in determining the suitability of these amplifiers for specific applications, considering factors such as power efficiency, noise sensitivity, and frequency requirements.

## d. Verification against Design Specifications:

The simulation results of the two amplifiers also serve as a means to verify if the design specifications and requirements have been met. By comparing the simulation results against the desired performance goals, researchers can assess the success of the design methodology and optimization techniques employed [3]. Any deviations or discrepancies between the simulation results and design specifications can be analysed to identify potential areas for further improvement or optimization.

Simulation results are critical for evaluating the performance of high-gain multistage CMOS amplifiers. Through simulation, researchers can assess the gain, bandwidth, noise characteristics, and power consumption of the amplifiers [8]. The simulation results enable comparative analysis between different amplifier designs and help verify if the design specifications have been met. By studying the simulation results, researchers can gain valuable insights into the performance of the two amplifiers and draw conclusions about their suitability for specific applications.

**VI. The different types of multistage amplifiers**.

Multistage amplifiers play a significant role in amplifying weak signals while maintaining desirable performance characteristics such as gain, bandwidth, and stability. This literature review focuses on exploring the various types of multistage amplifiers commonly used in analog
circuit design [20]. By examining the characteristics, advantages, and limitations of different multistage amplifier configurations, this review aims to provide a comprehensive understanding of the design choices available to engineers and researchers.

## a. Cascade Amplifiers:

Cascade amplifiers are one of the fundamental types of multistage amplifiers, where multiple amplifier stages are connected in a series configuration. Each stage amplifies the signal, and the output of one stage becomes the input of the next stage [4]. Cascade amplifiers offer several advantages, including high overall gain, low input/output impedance, and the ability to tailor each stage for specific performance requirements. However, cascade amplifiers may suffer from limited bandwidth and potential stability issues due to the accumulation of noise and parasitic effects.



**Figure I: Circuit diagram of Cascade Amplifiers [16]**

## b. Darlington Amplifiers:

Darlington amplifiers are a type of multistage amplifier that utilizes a Darlington pair, which consists of two bipolar junction transistors (BJTs) connected in a common-emitter configuration. The input of the first transistor is connected to the signal source, while the output of the first transistor becomes the input of the second transistor [3]. Darlington amplifiers provide high current gain, enabling efficient amplification of small input signals. They are commonly used in applications requiring high current drive capability, such as power amplifiers and audio amplifiers.



**Figure II: Circuit diagram of Darlington Amplifiers [20]**

## c. Cascode Amplifiers:

Cascode amplifiers combine two different transistor types, such as a common-emitter BJT and a common-gate field-effect transistor (FET), in a multistage configuration. The cascode configuration provides advantages like high gain, wide bandwidth, and improved stability compared to single-stage amplifiers [5]. The combination of a high-input impedance device (FET) and a low-output impedance device (BJT) helps minimize loading effects and enhances the overall performance of the amplifier. Cascode amplifiers are often used in applications requiring high gain and wide bandwidth, such as RF amplifiers and high-frequency signal processing.



**Figure III: Circuit diagram of Cascode Amplifier [23]**

## d. Distributed Amplifiers:

Distributed amplifiers are multistage amplifiers that utilize transmission lines or distributed components, such as inductors or capacitors, to achieve high gain and wide bandwidth. These amplifiers are commonly used in microwave and high-frequency applications, where distributed components can effectively handle the signal propagation and maintain a consistent gain across the frequency spectrum [9]. Distributed amplifiers offer high linearity, low noise figure, and excellent bandwidth, making them suitable for applications such as radar systems, wireless communications, and high-speed data transmission.

**Figure IV: Circuit diagram of Distributed Amplifier [22]**



## e. Operational Amplifiers:

Operational amplifiers (op-amps) are integrated circuit (IC) multistage amplifiers widely used in a range of analog and mixed-signal applications. Op-amps typically consist of multiple amplifier stages, including differential amplifiers, gain stages, and output buffers, integrated into a single chip [10]. These amplifiers offer high gain, high input impedance, low output impedance, and excellent linearity. Op-amps find extensive use in applications such as audio amplification, signal conditioning, instrumentation, and active filters.



**Figure V: Circuit diagram of Operational Amplifiers [21]**

Multistage amplifiers encompass various configurations, each offering distinct advantages and suitability for specific applications. Cascade amplifiers, Darlington amplifiers, cascode amplifiers, distributed amplifiers, and operational amplifiers represent a diverse range of multistage amplifier designs [15]. Understanding the characteristics, advantages, and limitations of these different types of multistage amplifiers enables engineers and researchers to select the most appropriate configuration for their specific design requirements.

# VII. Factors that affect the gain of a multistage amplifier:

The gain of a multistage amplifier is a critical parameter that determines its ability to amplify weak input signals. Understanding the factors that affect the gain of a multistage amplifier is crucial for optimizing its performance and ensuring desired output characteristics. This literature review focuses on exploring the key factors that influence the gain of a multistage amplifier, as identified by researchers [7]. By examining these factors, their impact on amplifier gain, and the proposed mitigation strategies, this review aims to provide a comprehensive understanding of the gain behaviour in multistage amplifier designs.

## a. Device Parameters and Characteristics:

The choice of active devices, such as transistors, significantly affects the gain of a multistage amplifier. Parameters like transconductance (gm), early voltage (VA), and output conductance (gds) play a vital role in determining the gain [15]. Higher transconductance and early voltage can lead to higher gain, while higher output conductance can reduce the gain. Researchers have explored device modelling, optimization, and selection techniques to enhance the gain performance of multistage amplifiers.

**Table V: Device Parameters and Characteristics**

|  |  |
| --- | --- |
| **Parameter** | **Description** |
| Transconductance (gm) | The ratio of the output current to the input voltage. |
| Output resistance (ro) | The resistance is seen at the output of a transistor. |
| Early voltage (Va) | The voltage at which the output resistance of a transistor begins to decrease. |
| Beta (β) | The ratio of the collector current to the base current. |
| Cutoff frequency (fT) | The frequency at which the gain of a transistor drops by 3dB. |
| Gain-bandwidth product (GBW) | The product of the gain and bandwidth of a transistor. |
| Noise figure (NF) | The ratio of the noise power output of a transistor to the noise power input. |
| Power consumption (P) | The amount of power that a transistor consumes. |

## b. Load and Source Impedances:

The load and source impedances connected to the multistage amplifier can impact its gain. Proper matching of load and source impedances helps maximize power transfer and minimize reflections [2]. Mismatches in impedance can result in gain reduction or distortion. Techniques such as impedance-matching networks and careful selection of load and source components are employed to mitigate impedance-related gain losses.

**Table VI: Load and source impedance**

|  |  |
| --- | --- |
| **Parameter** | **Description** |
| Load impedance (ZL) | The impedance is seen at the output of a circuit. |
| Source impedance (ZS) | The impedance is seen at the input of a circuit. |
| Impedance matching | The process of ensuring that the load and source impedances are well-matched. |
| Maximum power transfer | The maximum power that can be transferred from a source to a load is achieved when the load impedance is equal to the source impedance. |
| Reflection coefficient (Γ) | The ratio of the reflected wave to the incident wave. |
| Standing wave ratio (SWR) | The ratio of the maximum voltage to the minimum voltage in a transmission line. |

## c. Frequency-Dependent Gain:

Multistage amplifiers often exhibit frequency-dependent gain characteristics due to parasitic capacitances, inductances, and the presence of reactive components. These factors introduce frequency-dependent voltage gain and phase shifts [12]. Researchers have investigated techniques such as frequency compensation, pole-zero placement, and compensation capacitors to achieve consistent gain across the desired frequency range and maintain stability.

**Table VII: Frequency-dependent gain**

|  |  |
| --- | --- |
| **Parameter** | **Description** |
| Frequency-dependent gain (f-d gain) | The gain of a circuit that varies with frequency |
| Gain roll-off | The decrease in gain with increasing frequency. |
| Bandwidth | The range of frequencies over which the gain of a circuit is within a specified range. |
| Passband | The frequency range over which the gain of a circuit is constant. |
| Stopband | The frequency range outside of the passband where the gain of a circuit is very low. |

## d. Power Supply Variations:

Power supply variations can impact the gain of a multistage amplifier, particularly in the presence of active biasing circuits. Variations in power supply voltage can alter the bias points of the amplifier stages, leading to gain deviations [18]. Researchers have explored robust biasing techniques, feedback mechanisms, and adaptive biasing schemes to mitigate the impact of power supply variations and maintain stable and consistent gain.

**Table VIII: Variations of power supply**

|  |  |
| --- | --- |
| **Parameter** | **Description** |
| Power supply variation (PSV) | The change in the voltage of a power supply over time. |
| Noise | Random fluctuations in the voltage of a power supply. |
| Dips | Sudden drops in the voltage of a power supply. |
| Sags | Slow decreases in the voltage of a power supply. |
| Swells | Slow increases in the voltage of a power supply. |

## e. Parasitic Effects:

Parasitic elements, such as parasitic capacitances, inductances, resistances, and stray capacitances, can introduce undesirable effects in multistage amplifiers. These parasitic can degrade the gain, introduce stability issues, and impact overall amplifier performance [17]. Researchers have proposed various techniques, including layout optimization, isolation structures, and shielding, to minimize parasitic effects and preserve the gain of multistage amplifiers.

# VIII. The trade-offs between gain, noise figure, bandwidth, and power consumption in high-gain amplifier design

Designing high-gain amplifiers involves trade-offs between various performance metrics, including gain, noise figure, bandwidth, and power consumption. Achieving high performance in all these aspects simultaneously can be challenging due to conflicting design requirements [14]. This literature review focuses on exploring the trade-offs encountered in high-gain amplifier design and the approaches proposed by researchers to strike a balance between gain, noise figure, bandwidth, and power consumption. By examining these trade-offs, this review aims to provide insights into the optimization strategies employed to achieve desired amplifier performance.

## a. Gain versus Noise Figure:

The gain of an amplifier is essential for amplifying weak input signals, while the noise figure characterizes its ability to maintain signal integrity by minimizing added noise. Increasing gain often leads to higher noise figures due to the inherent noise contributions of active devices and resistive elements [3]. Researchers have investigated various noise optimization techniques, careful transistor sizing, and low-noise design methodologies to mitigate noise figure degradation while maximizing gain.

**Table IX: Gain versus Noise Figure**

|  |  |
| --- | --- |
| **Parameter** | **Description** |
| Gain | The ratio of the output signal power to the input signal power. |
| Noise figure (NF) | The ratio of the noise power output of a circuit to the noise power input. |
| Noise temperature (Tn) | The effective temperature of the noise added by a circuit. |
| Noise bandwidth (Bn) | The frequency range over which the noise power of a circuit is significant. |

## b. Bandwidth versus Gain:

Amplifiers with wide bandwidth are desirable for applications requiring high-speed signal processing. However, achieving wide bandwidth while maintaining high gain can be challenging due to the increased parasitic capacitances and the resulting gain-bandwidth product limitations [9]. Researchers have explored techniques such as cascode configurations, active feedback, and current reuse to extend the bandwidth of high-gain amplifiers without compromising gain performance. Additionally, the use of novel circuit topologies and advanced compensation techniques has been proposed to overcome bandwidth limitations.

## c. Power Consumption versus Gain:

Power consumption is a critical consideration, particularly in portable and low-power applications. High-gain amplifiers typically consume more power due to larger bias currents and multiple gain stages. Minimizing power consumption while maintaining the desired gain is a trade-off that researchers have addressed through various low-power design strategies. These strategies include bias current reduction, subthreshold operation, and supply voltage scaling [4]. Optimization algorithms and design methodologies that consider power consumption as a key design metric have also been proposed to achieve power-efficient high-gain amplifiers.

## d. Gain-Bandwidth Trade-Offs:

The gain-bandwidth trade-off is a fundamental consideration in high-gain amplifier design. Increasing the gain often results in reduced bandwidth due to the limited gain-bandwidth product of active devices [2]. Researchers have explored various techniques, such as cascading multiple gain stages, employing frequency compensation methods, and optimizing transistor sizing, to balance the gain-bandwidth trade-off. These approaches aim to achieve optimal gain and bandwidth performance based on specific application requirements.

# IX. Conclusion

The review of high-gain multistage CMOS amplifier design at the 45nm technology node highlights the challenges and advancements in designing high-performance amplifiers at this advanced technology node. Several key aspects have been discussed, including noise optimization, stability enhancement, bandwidth limitations, and power consumption [8]. Researchers have addressed the challenges by employing techniques such as noise optimization at each stage, careful transistor sizing, low-noise design methodologies, and advanced noise-cancellation techniques. Stability has been enhanced through compensation techniques like pole-zero placement, Miller compensation, and dominant pole compensation. Bandwidth limitations have been tackled with cascode configurations, active feedback, current reuse, and exploration of novel topologies. Power consumption has been optimized using bias current reduction, subthreshold operation, and supply voltage scaling. Simulation results have played a crucial role in evaluating the performance of the designed amplifiers. They have provided insights into gain, bandwidth, noise figure, and power consumption. Comparative analysis between different amplifier designs has allowed researchers to assess the effectiveness of various approaches and verify if design specifications have been met. The review has shed light on the importance of device parameters, load/source impedances, frequency-dependent effects, power supply variations, and parasitic elements in determining the gain of multistage amplifiers. Understanding these factors and their impact on gain has enabled researchers to optimize amplifier performance.

Overall, the review emphasizes the significance of research efforts in overcoming challenges and achieving high-performance multistage CMOS amplifiers at the 45nm technology node. Further advancements in device technologies, modelling techniques, and circuit design methodologies will continue to contribute to the development of high-gain amplifiers for various analog integrated circuit applications at advanced technology nodes.

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