**Characterizing Charge Plasma-based Junctionless TFETs for Biosensors**

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**Abstract—** This chapter aims to examine and characterize charge plasma-based junctionless TFETs for biosensor devices. Despite the device's obvious benefits, the steep doping profile associated with classic Tunneling Field Effect Transistor (TFET) poses significant production issues. Les TFETs sans junction (JL-TFETs) réduisent considérablement le problème en offrant un profil de dopage constant à travers le dispositif. In this study, we examined several device variables that affect device performance. These included gate insulator dielectric constant, gate insulator thickness, silicon body thickness, doping level, P-gate and source work function. La recherche se concentre sur les paramètres qui ont un impact sur le swing sous-threshold (SS), la proportion d'énergie à énergie hors-énergie (Ion/Ioff) et la tension sous-threshold (VT). Additionally, the impact of different parameters on the on-current (Ion) has been studied. Nous avons pu déterminer comment l'ajustement des paramètres peut entraîner une performance maximale du système grâce à ces informations.

***Keywords*:** Junctionless TFET, Sub threshold Swing, Work Function, Threshold Voltage, Non-local Band-to-Band Tunneling Model

**I. INTRODUCTION**

Field-effect transistors (FETs) have enhanced biosensing technology by increasing sensitivity, reliability, and compactness. Junctionless tunneling FETs (TFETs) are promising due to their ultra-low power consumption and increased performance.

The advantages of charge plasma-based junctionless devices are being studied to better understand the intricate interplay between TFETs and biosensing. This study examines their electrical properties and sensitivity in order to enhance biosensor development.

Years of aggressive MOSFET scaling have resulted in an unfavorable rise in short channel effects, leakage current, and MOSFET subthreshold swing is also limited to 60 mV/dec [1]. As a result, substantial research is being conducted in order to find alternative technologies. One of the most promising of these devices is the tunneling field effect transistor (TFET) [2-4]. TFETs exhibit substantially lower sub threshold swing than MOSFETs due to the band-to-band tunneling process [5-7]. TFETs also have reduced leakage current, ultra-low power dissipation, and very low off current due to their large tunneling barrier in the off state. However, the fabrication of TFETs necessitates a high doping concentration and an asymmetric doping structure, posing a significant barrier to our research's current fabrication method [8]. However, such concerns can be solved using junctionless TFETs (JL-TFETs), which use the charge-plasma principle to generate a P-I-N doping configuration in a uniformly doped silicon device [9-10].

**II.JUNCTIONLESSTFET DEVICE STRUCTURE**

A junctionless TFET (JL-TFET) is constructed in the same manner as a regular TFET, except that instead of p-i-n doping, a uniformly doped silicon body wafer is employed. Work function engineering is used to create the p-i-n doping profile in the structure. As a consequence, the cost and complexity of doping throughout the manufacturing process can be reduced. The JL-TFET is depicted schematically in Fig. 1. The source, gate, and drain electrode work functions were tuned to 5.40 eV, 4.20 eV, and 3.90 eV, respectively. Furthermore, the work function of the P-Gate (gate above the source region) is 5.40 eV. The silicon body thickness is 10 nm, the dielectric thickness is 3 nm, and the gate insulator dielectric constant is 7. The silicon body contains 1018cm3 of homogeneous n-type doping. The parameters listed above are maintained constant while the parameter of interest is modified. It should be noted that a high-spacer of 5 nm (k =21) is employed. The P-gate is 20 nm in length, whereas the control gate is 25 nm in length. VDS has been set to 1 V in this investigation for all simulation types.



**Fig. 1.** Device Schematic of JL-TFET.

In the ON state, the creation of a p-i-n region may be detected, as shown in Fig. 2. The appropriate work function selection has a significant influence on JL-TFET performance [12].



**Fig. 2.** A Graph of carrier concentration (*κ*=16) in the ON state.

Fig. 3 shows a transfer curve of a JL-TFET (=16 for gate insulator) with VGS swept from 0 V to 2 V.



**Fig. 3.** Transfer curve of a JL-TFET.

**III. METHODOLOGY**

A non-local band-to-band tunnelling model is utilized to simulate the device, which takes into consideration the tunneling process's intrinsic non-locality. Fermi-Dirac statistics, concentration-dependent mobility, bandgap narrowing, trap-assisted tunneling (TAT), Auger recombination, and Shockley-Read-Hall rearrangement (SRH) are also employed. The intrinsic carrier concentrations necessary to assess SRH recombination are calculated using Fermi Statistics. To answer numerical problems, the Newton technique is applied.

**IV. SIMULATION RESULT**

***A. Effects of κ on JL-TFET***

To investigate the influence on JL-TFET, we altered the dielectric constant of the gate insulator as follows: SiO2 (=3.9), Si3N4 (= 7), and Y2O3 (= 16). We determined that increasing the dielectric constant minimizes the sub threshold swing, as seen in Fig. 4. These findings are comparable with those of Ghosh et al. and Bal et al. in their research reported in [10] and [11-12], respectively. These benefits are attributable to the increased gate coupling ability of high-insulators. Ion is more controllable due to its increased gate controllability.



**Fig. 4**. SS improves as *κ* increases.

Improves notably when high-*κ* gate dielectric is used resulting in improvement of I*ON*/I*OFF* ratio as illustrated in Fig. 5.



**Fig. 5.** I*ON*/I*OFF* increases significantly with the increase of *κ*.

As seen in Fig. 6, raising the threshold voltage improves performance. Despite the significant variation in current due to changes in some parameters, the constant current approach uses 109A/m as the current to establish the threshold voltage. Our research also shows that employing high-quality materials can lead to enhanced performance. This is congruent with the findings of the [13] research.



**Fig. 6.** V*T* and *κ* have negative correlation.

**B. Effects of doping level in JL-TFET**

Table I shows how the doping level is varied in order to examine the effect of doping level. An rising or decreasing pattern of Ion and VT may be detected as the amount of doping rises. Even if increasing doping levels result in little gains, it should be remembered that the impacts of doping levels are not as important as other criteria. The generally low on-current values are due to the low and high tins employed during parametric variation.

TABLE IEFFECTS OF DOPING LEVEL ON I*on* AND V*T*

|  |  |  |
| --- | --- | --- |
| **Doping level (/cm3)** | **I*on* (*A/μm*)** | ***VT* (V)** |
| 1017  | 4*.*61 *×* 10*−*8 | 1*.*30 |
| 1018 | 4*.*63 *×* 10*−*8 | 1.29 |
| 1019 | 5.65 *×* 10*−*8 | 1.24 |
| 1020 | 6*.*61 *×* 10*−*8 | 1.22 |

***C. Effects of P-Gate and Source work function on JL-TFET***

We've seen how work function affects device performance. Table II illustrates how on-current and threshold voltage vary as the work function varies. As illustrated in Fig. 7, the ion rises as the energy barrier width increases, resulting in higher tunneling current. Furthermore, the work function is inversely proportional to the threshold voltage.

**TABLE II EFFECTS OF P-GATE AND SOURCE WORK FUNCTION ON I*on* AND V*T* .**

|  |  |  |
| --- | --- | --- |
| ***φ* (eV)** | **I*on* (*A/μm*)** | ***VT* (V)** |
| 5*.*50 | 4*.*61 *×* 10*−*8 | 1.22 |
| 5.60 | 3*.*25 *×* 10*−*8 | 0.98 |
| 5.70 | 1*.*22 *×* 10*−*8 | 0.66 |



**Fig. 7.** Band diagram for different work function values.

**V. CONCLUSION**

JL-TFET is one of the most well-known TFET modifications because it may overcome the restrictions that are typically encountered in standard TFET manufacturing. In this investigation, we observed that using a high-gate dielectric increased the performance of the JLTFET device. Tin reduction boosts SS, Ion/Ioff, and VT. Furthermore, as the thickness of the silicon body reduces, so does Ion and VT. Furthermore, an increase in doping level can enhance Ion and VT, albeit the effects are minor. The engineering of gate work functions has a substantial influence on both Ion and VT. Our findings can help in the selection of settings for the optimal device performance in JL-TFETs.

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