**Design of Thin film CdTe Solar Cell using PC1D**

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**1. Introduction:**

* 1. **Need for sustainable energy source**

The world energy requirement is ever growing, particularly since last few centuries. It is expected to grow further in future. The main reason of energy demands are (a) growth in world population and (b) the techno- economic growth of the countries. The increasing energy demands puts a a lot of pressure on conventional energy sources (e.g. oil, gas, coal). But since fossil fuels are limited in quantity and cause environmental pollution. Hence there is a need for alternative energy sources which can provide us energy in sustainable manner. The obvious choice of a clean energy source, which is abundant and could provide sustainable energy is sun’s energy.

* 1. **Sun’s energy: Advantages:**

Following are the advantages of using sun’s energy:

* It is everlasting, renewable energy source.
* It is clean energy source, no potential damage to the environment.
* It is very large source energy. The power from the sun receivied by earth is about 1.8 ×1011MW which is many thousand times larger than energy currently found from all other sources.
* Solar energy is free available to everywhere, doesn’t cause any pollution.
  1. **Solar cell and its basic operational principle:**

Sunlight can be converted to electricity due to the photovoltaic effect discovered in 1839 by Edmund Becquerel, a French Scientist. Sunlight is composed of photons, or packet of energy. These photons contain various amounts of energy corresponding to the different wavelengths of light. When photons strike a solar cell, a semiconductor P-N junction device, they may be reflected or absorbed or they may be passed though the cell. Absorption of a photon in a solar cell results in generation of electron-hole pair(EHP). These EHP when separated from each other across the P-N junction, results in the generation of a voltage across the junction, which can drive the current in an external circuit and hence power can be extracted from the solar cell or photovoltaic (PV) cell.

The working principle of all today solar cells is essentially the same. It is based on the photovoltaic effect. In general, the photovoltaic effect means the generation of a potential difference at the junction of two different materials in response to visible or other radiation.

The basic processes behind the photovoltaic effect are:

1. Generation of the carriers due to the absorption of photons in the materials

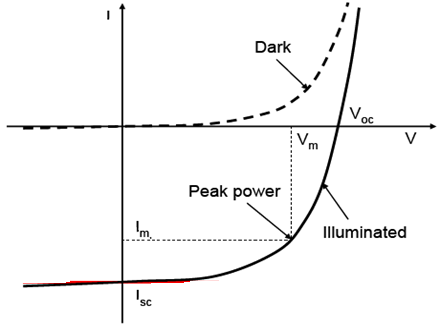
2. Subsequent separation of the photo-generated carriers (EHP) in the junction

3. Collection of the photo-generated charge carriers at the terminals of the junction.

In general, a solar cell structure consists of an absorber layer, in which the photons of an incident radiation are efficiently absorbed resulting in a creation of electron-hole pairs. In order to separate the photo-generated electrons and holes from each other, the so-called “semi-permeable membranes” are attached to the both sides of the absorber. The important requirement for the semi-permeable membranes is that they selectively allow only one type of charge carrier to pass through. An important issue for designing an efficient solar cell is that the electrons and holes generated in the absorber layer reach the membranes. This requires that the diffusion lengths of the charge carriers are larger than the thickness of the absorber.

**1.4 Current voltage parameters under illumination:**

The analysis of the solar cell behavior is done by examining the tree main parameters namely thee *“open circuit voltage”* **VOC**which is the voltage under the condition in which the impedance of the device is lesser than the load, the *“short circuit current”* **ISC** which is the current when the impedance of the device is greater than the load and the *“fill factor”* **FF**, which is defined as the ratio of the maximum power output to the product of the open circuit voltage and short circuit current. Now the efficiency **η** of a solar cell is defined as the ratio of maximum/peak power output to the input power. The I-V curve of solar cell is given in figure 1 under dark and illumination.



**Fig.1** : Light and dark curves for solar cell

**1.5 An overview of CdTe Solar cell:**

Since beginning, the dominant solar cell technology in the marketplace has been based on wafers of crystalline silicon. These cells are made with bulk crystals, often recycled from the microelectronics industry. Because of the particular process to produce them, crystalline and multi crystalline silicon cells have still too high cost to be considered as a reasonable competitor to the energy production from fossil fuels. In the later period, the idea of developing alternative, lower cost PV technologies led to the consideration of thin films. Thin film solar cells have two advantages: the amount of material used is very small and the production processes involved are easily scalable. For these reasons it is calculated that the average cost per watt of a thin film solar cell would be less than that of the silicon solar cell. Thin films are based on using thinner semiconductor layers of few microns to absorb and convert photon. The first thin film technology which has been developed from the day of inception and was manufactured was made op of amorphous silicon. However, this technology has not being able to become a market leader since it suffers from low efficiencies and slow deposition rates. Rather, the PV market has now grown with wafer-based crystalline silicon. Now a days, two other thin films continued to be challenging the Si development (Cadmium Telluride, and Copper Indium Gallium diselenide or CIGS-alloys). Heterojunctions solar cell based on CdTe have been considered since the early 1960s, for thin-film devices on a glass substrate has also been investigated. CdTe is very easy to grow and it has a band gap (about 1.5 eV) almost perfectly matched to the absorption of photons in the solar spectrum in terms of optimal conversion to electricity. Now-a-days Cadmium Telluride (CdTe) is a promising photovoltaic material for thin-film solar cells and plays a key role in today’s fast growing photovoltaic industry. CdTe thin film solar cells have shown high potential for low cost photo voltaic energy conversion. However, the performance and reproducibility of devices has been limited by the conventional SnO2/CdS/CdTe device structure used for more than 30 years. Thin-film cadmium telluride (CdTe) solar cells are the basis of a significant technology with major commercial impact on solar energy production.

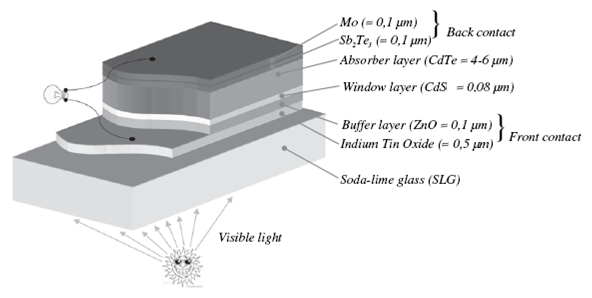
CdTe exhibits a forbidden gap of 1.45 eV very close to the maximum for solar energy conversion. Also its gap is direct and its absorption coefficient is in the range of 104 - 105 cm-1 for photon energies larger than the forbidden gap. This means that only a few micrometers of material are enough to absorb all the light. A theoretical maximum efficiency over 27% and a practical efficiency of 18.5% could be expected for this material with an open-circuit voltage of 880 mV and a short-circuit current density of 27 mA/cm2 (with a negligible thin layer of CdS). CdTe is one of the few II-VI compounds that can be prepared both p- and n-type.

**1.6 Different layers of CdTe/CdS solar cell:**

The schematic structure of today’s typical CdTe/CdS polycrystalline thin film solar cell is shown in Fig. 2. The cells are in the super-strate configuration, with light coming to the junction through the substrate.

The substrate can be soda-lime glass (the common window glass) or special alkali free glass. The choice of alkali-free glass assures no diffusion of pollutants species into the overhanging films and allows more freedom in cell processing, having a higher softening temperature.

The front-contact layer is commonly made of a TCO such as indium tin oxide (ITO), fluorine doped indium oxide(IFO) or fluorine doped tin oxide(FTO). On top of this electrical conductive layer are often deposited a few nanometers (50-200) of a buffer layer such as pure TO, ZnO or Ga2O3 which has the role of a shield against the probable diffusion of Na and K atoms. Generally, these layers are rather resistive showing electrical resistivity in the range of 102-105 Ω-cm; for this reason they are also effective in preventing an increase of the junction reverse saturation current if some pinholes are present in the subsequent very thin CdS film.



**Fig. 2**: Schematic of the CdTe/CdS solar cell structure.

The window layer, that is the CdS film, represents the n-type part of the junction. In highly efficient CdTe based solar cells the CdS films are deposited either by Close-Spaced Sublimation (CSS) or by sputtering. In order to maximize the solar cell photocurrent it is necessary to minimize the CdS film thickness and this is helped by the buffer layer presence between the CdS and the TCO films. Typical CdS layer thickness is in the range of 70 to120 nm.

In efficient CdTe/CdS solar cells, CSS is the most popular technique used to deposit 4-7 μm thick CdTe films which is on top of CdS as per figure 2. This deposition method is particularly suitable for large-scale application since it is very fast (only 1 or 2 min are needed). Best cell performance is obtained if the CdTe films are grown in an oxidizing atmosphere. After this layer there is back contact

**2. Review of CdTe Solar Cells**

* 1. **High-Efficiency Polycrystalline CdS/CdTe Solar Cells:**

Difference in efficiencies between commercial modules and lab-scale cells are dominant throughout the solar industry. The CdS/CdTe solar cell has a maximum theoretical efficiency of approximately 30%, with a more conservative practical limit of around 20%. The industry leader in CdTe solar now reports record module efficiencies of 13.4% and a record lab-cell efficiency of 17.3%.EPIR’s best device demonstrated an NREL-verified efficiency of 15.3%. The mean efficiency of hundreds of cells produced with a buffer layer between December 2010 and June 2011 is 14.4%. Quantum efficiency results are presented to demonstrate EPIR’s progress toward NREL’s best-published results.

Multiple polycrystalline CdS/CdTe solar cells with efficiencies greater than 15% were produced on buffered, commercially available Pilkington TEC Glass at EPIR Technologies, Inc. (EPIR, Bolingbrook, IL) and verified by the National Renewable Energy Laboratory (NREL). n-CdS and p-CdTe were grown by chemical bath deposition (CBD) and close space sublimation, respectively.

EPIR’s results for cells on commercial glass were obtained by implementing a high-resistivity SnO2 buffer layer and by optimizing the CdS window layer thickness. The high-resistivity buffer layer prevents the formation of CdTe-TCO junctions, thereby maintaining a high open-circuit voltage and fill factor, whereas using a thin CdS layer reduces absorption losses and improves the short-circuit current density.



**Fig. 3:** I–V curve and derived parameters of an NREL-verified,EPIR-produced, high- efficiency polycrystalline CdTe solar cell.

Using a series of focused process optimizations, EPIR has produced multiple polycrystalline CdS/CdTe solar cells on commercially available TCO coated glass with efficiencies above 15%. The best device without an antireflection coating (ARC) exhibited an NREL-verified efficiency of 15.3%. The I–V characteristic and measured device parameters for this cell are shown in Fig. 3. The implementation of a buffer layer has been crucial in achieving these results.

Demonstrating good performance in a single cell is important as a proof of concept for the possibility of improving module efficiencies, but obtaining uniformly high-performance cells is also a primary 1concern. The mean efficiency of all of the hundreds of cells produced at EPIR with a buffer layer between December 2010 and June 2011 is 14.4%.

**2.2 Ultra-thin CdTe solar cells using MOCVD:**

A study was made on very thin CdTe absorber < 1 μm layers to investigate limitations in CdTe collection efficiency. In order to reduce material usage and to address carrier recombination loss throughout the absorber layer, the CdTe absorber thickness has been decreased below the absorption limit of 1 μm. The absorber layer thickness for thin film CdTe solar cells is normally between 2 and 10 μm. Thicker absorber layers are generally used to avoid pinholes reaching through to the window layer, which may lead to shorting from the back contact.



**Fig. 4**: Light J–V curves (under 100 mW/cm2 xenon lamp illumination) for i) 0.5 μm, ii) 1 μm and iii) 2 μm absorber thicknesses.

J–V measurements of thin and ultra thin absorbers can be used to investigate voltage dependent collection in devices. It, it is suggested that the reduction of the absorber layer thickness increases the voltage dependent collection at high forward bias. Above figure shows the light J–V curves for different absorber layer devices. The open circuit voltage (Voc) is seen to increase with absorber thickness, due to an increase in the photo generated current (JL) as the absorption volume is increased. Evolution of series resistances with absorber thickness, shows minimal change in series resistance, demonstrating that the back contact barrier is unaffected by the close proximity of the pn junction, even down to 200 nm absorber thickness. A large decrease in shunt resistance (approximated from J–V curves) with decreasing absorber thickness is observed. Such increase in shunting is possibly caused by leakage currents around the edges of the cell, as the layers are so thin, but it could also be due to extended lattice defects (grain boundaries, dislocations, etc …) in the depletion region of the device. Dark J–V (fig 5) have also been measured and show recombination effects are increased for the 500 nm thick CdTe layer in the reverse bias region. The dark J–V curves shows that when the absorber thickness is reduced below the CdTe absorption thickness (~1 μm), recombination effects increase and dominate device characteristics.



**Fig. 5**: Dark J–V curves of cells with different absorber thickness showing increased recombination for the thinner cells.

The large decrease in device parameters with decreasing absorber thickness (below 1 μm) suggests the cells are limited not only by optical issues but also interface and possibly back contact proximity. By the basic addition of an acceptor defect between the CdS and CdTe, the agreement of the basic model with measured results improved, particularly when ultra thin absorbers were employed, possibly signifying an increase in the interface defect density with thinner absorbers.

**2.3 Thin-film CdTe cells - reducing the CdTe:**

CdTe as polycrystalline thin-film material is currently the dominant thin-film technology in global photovoltaic manufacturing. Having finite resources of Te available in world-wide, it is required to consider the idea to reduce the thickness of the CdTe material for these devices. Many advantages accumulate from reducing the absorber layer thickness in solar cells direct bandgap materials such as CdTe which include less use of materials particularly low earth abundance materials such as In and Te with reduced post-deposition processing time, reduced deposition time and lower potential environmental impacts. Semiconductor absorber materials with direct bandgap rarely need thickness higher than one micron to absorb full light beyond a few meV of the band edge. CdTe is normally fabricated in the superstrate structure and interestingly back-contact processing may limit CdTe thickness reductions. This may happen due to the chemical etch process, such as nitric–phosphoric acid, that predominantly etches down grain boundaries and may lead to excessive shunting as we move towards CdTe thickness reduction.



**Fig. 6**: Different J–V characteristics of solar cells with different CdTe thickness.

The CdTe thicknesses were chosen as: 0.3 μm, 0.5 μm, 0.65 μm, 0.8 μm, 1.1 μm, 1.45 μm, 1.85 μm, 2.2 μm and 2.6 μm. Above 1.1 μm, the J–V characteristics are nearly not very dependent of CdTe thickness. Above figure shows the J–V characteristics of the five different thin cell structures. A continuing drop with CdTe thickness is considered at the same time drop in all primary cell parameters, VOC, JSC, and FF also observed.



**Fig. 7**: Maximum and average cell efficiencies with respect to the CdTe thickness.

It is noticable that 12% efficiency is achieved at 1.1 μm and 9.7% at 0.5 μm.



Fig. 8: QE vs. bias of 1.1 μm and 0.5 μm cells.

External QE is shown in Fig. 8 for five different bias voltages (0.4 V, 0.3 V, 0 V, -0.5 V and −1 V). Very little voltage dependent collection is observed at higher thickness of CdTe, Fig. 8 shows a strong (0.5 μm) and moderate (1.1 μm) dependence of current collection at forward biases of 0.5 and 0.4 V respectively. This behaviour is observed for the thinner cells that when the CdTe is not fully depleted, e.g., at +0.4 or +0.5 V and when applied strong electric field is reduced, the minority carrier collection becomes poor. This is caused by the back contact The reasons of reduced absorber minority carrier lifetime caused by the back contact interface and Cu recombination centres close proximity of the back contact.

**3. Design of High efficient CdTe solar cell using PC1D:**

**3.1 Introduction:**

As far as cost effective and reliable photovoltaic cells are concerned polycrystalline thin film CdTe is becoming a leading material for the industry. The most attractive properties due to which it is in focus are its band gap (1.5 eV) which is close to the ideal one (1.45 eV) and its high optical absorptivity. Hetero-junctions thin film CdTe solar cells typically use CdS as its window layer. Efficiencies as high as 16.5% have been achieved so far, but still there is provision to increase.

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**Fig. 9:** Schematics of a typical superstrate CdS/CdTe solar cell structure.

As it is observed in Fig. 9, the typical four layer structure of a CdTe/CdS solar cell as given below:

1. Transparent and Conducting Oxide (TCO) which acts as a front contact,

2. Window layer of CdS film is the so called,

3. Absorber layer of CdTe film which is the made on top of CdS;

4. The back contact on top of the CdTe layer.

The TCO characteristics that must possess to become a front contact for the thin-film CdTe/CdS solar cells are:

* High degree of transparency greater than 85% in the wavelength region of interest (400–900 nm).
* Low resistivity in the order of 2 × 10-4 Ω-cm.
* Good stability at high temperature at which other layers are stacked which means that there should not be any diffusion from transparent conductive oxide layers to the other subsequent layers.

For high-efficiency low cost thin film polycrystalline solar cells. CdTe is a direct bandgap material CdTe is an ideal absorber material with an energy gap of 1.5 eV with an absorption co-efficient around 104 cm-1 in the visible region, which means that few micrometers layer thickness of is sufficient to absorb 90% of the incident photons.

**3.2 PC1D overview:**

PC1D is a computer program which runs on all 32-bit MS Windows operating systems. PC1D utilizes the drift-diffusion model which is one-dimensional. It solves the nonlinear equations for transport of electrons and holes in the quasi-one-dimensional structure in crystalline semiconductor devices, with emphasis on photovoltaic devices. The program was initially written at Sandia National Labs by Dr. Paul Basore and coworkers and was further developed by Dr. Don Clugston at the University of New South Wales, Australia. The emphasis has been given to convergence for a broad range of doping profiles considering boundary conditions. Since its launch in 1982, it has undergone substantial improvements in terms of performance and capabilities. Its popularity is accredited to a user friendly interface, versatility of feeding and extracting data, and an extensive comprehension of parameters to accurately model solar cells.

It is important for all simulation programs to keep pace with the new developments in the experimental work and theoretical models in their domain. The last release of PC1D was version 5.9 in 1997. PC1D was primarily developed to model crystalline and polycrystalline silicon device structures, and addresses the properties that affect performance of common semiconductors like Si and GaAs. Thus, new materials such as the III-nitrides, i.e., Aluminium nitride (AlN), Gallium nitride (GaN) and Indium nitride (InN) and their alloys that offer substantial potential to develop high-efficiency solar cells, cannot be modeled using PC1D as it gives rise to inaccurate design rules and efficiency expectations. In this work, we present a descriptive model for polarization, a unique property of the III-nitride materials, and incorporate the effects of polarization into PC1D to study the effect that polarization would have on the design of solar cells developed using the nitrides.

**3.3 Program Description**

PC1D is a computer program solves the fully coupled nonlinear equations for transport of electrons and holes in the quasi-one-dimensional structure of crystalline semiconductor devices, with emphasis on photovoltaic devices initially written for IBM-compatible personal computers but now compatible with any PC. PC1D runs under Windows 95/98/ME/XP/NT and also in higher versions.

Only one file PC1D.EXE is necessary to run the program. The additional file PC1D.HLP provides on-screen help, and several additional files are provided which contain material parameters for selected semiconductors, standardized solar spectra, and example problems. All of the files can be simply copied into the directory of choice. To store files of different type in different directories, one needs to see the instructions for the Options menu.

**3.4 Few important options of PC1D:**

**3.4.1 Device Menu:**

The Device menu provides four different group selections as follows:

Region Manager: This selection allows us to manipulate the region numbers in our device. Regions can be made with different material with diffrent parameters.

Region Parameters: This portion only gives the current region. They allow us to examine and modify the thickness, material, doping, and recombination parameters.

Device Parameters: This group of selections allows changing the device parameter as a whole. Few areas are like modify the area of the device, surface texture, surface charge, external circuit contact locations, and the optical reflectance, both external and internal.

Device Files: This section allows us to create, retrieve, and store device files, having a suffix .DEV. These contain all of the information about the device only, without any excitation or numerical solution data.

|  |  |
| --- | --- |
|  |  |

**3.4.2 Excitation Menu**

The excitation menu offers the following commands:

Mode: This command allows us to control whether excitation to be applied steady-state or transient.

Temperature: This command allows us to set the device temperature in either Kelvin or degree Celsius. This temperature also has the effect to the carrier mobilities, surface recombination, optical absorption etc.

Base/Collector Source Circuits: These commands allow specifying the Thevenin-equivalent circuits for the base and collector. These circuits are only active if base and collector contacts have been enabled for the device.

Photo generation: This selection allows us introduce photo generation in the device. From a primary or secondary light source illumination can be provided, or the photo generation profile can be supplied from an external file.

Excitation Files: This set of commands help to create, retrieve, or store binary files that include all of the parameters essential to define the excitation. These excitation files, with suffix EXC, can then be used with a variety of different devices. Since the earlier versions, the graph definitions may be saved in excitation files. one toolbar button option is given to open the dialog box for retrieving a previously defined excitation file.

**3.4.3 Graph menu commands:**

The Graph menu provides commands that controlling and resetting the graphs in the Interactive-Graph view.

Spatial Graphs: This section provides choices menu for graphs that display spatial information. If the required information is not included in the list, more functions are available for a Defined Graph.

Temporal Graphs: This section provides the choices for graphs that display temporal information.

Defined Graph: This section form available 75 functions allows us to specify x and y functions for any graph. Detailed look at the operation of the device being provided by these functions.

Auxiliary Graph: This command deals with spatial function and a position within the device. From the Temporal Graph menu the data can also be viewed using the Auxiliary selection.

Experimental: This command opens a dialog box for data selecting from an external file. The data can be viewed on a user-defined graph with “Experimental Data” as one of the data types.

Previous and next History Graph: Once the simulation is completed, the current interactive graph is saved upto a maximum of 100 graphs. ‘History’ graphs can be viewed using the Graph menu or the Page Up/Down keys.

Simulation results can be compared by flipping through these graphs.

**3.5 Improvement of the efficiency of CdS/CdTe solar cells:**

Thickness of CdTe and CdS has been changed separately to check the improvement of cell efficiency in PC1D simulator. At first let us check the impact of CdS thickness variation.

**3.6 Variation of CdS thickness:**

Impact of window layer thickness to the performance of the cell has been studied.

**Table 1:** Performance values for different CdS thickness values

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| CdTe(μm) | CdS(μm) | Voc(V) | Isc(mA) | FF(%) | η(%) |
| 3 | 0.025 | 0.7524 | 28.6 | 85.04254916 | 21.51864 |
| 3 | 0.05 | 0.7518 | 28.6 | 84.64533604 | 21.50148 |
| 3 | 0.1 | 0.7506 | 28.7 | 84.02105261 | 21.54222 |
| 3 | 0.2 | 0.7475 | 28.9 | 82.85982109 | 21.60275 |
| 3 | 0.5 | 0.7398 | 29.3 | 80.27259466 | 21.67614 |
| 3 | 1 | 0.7289 | 30 | 78.65733754 | 21.867 |



**Fig. 10:** I-V characteristics of CdTe/CdS solar cell with CdS thickness 1 μm

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**Fig. 11:** QE-Wavelength curve of CdTe/CdS solar cell with different CdS thickness

Now it observed from above figure that there is not much change in FF and efficiency. It is observed from the above characteristic curves that efficiency is increasing if CdS thickness is increased. Carriers generated in the CdTe are collected and contribute to the photocurrent, while those in the CdS are lost. To allow above-gap optical transmission thin CdS of 50 - 100 nm, is therefore preferred. At the same time 1-10 μm thick CdTe gives homogeneity.

It will be difficult to substitute CdS as the window layer in this kind of solar cells since this material has shown that it forms an excellent hetero-junction with CdTe. Therefore, we can improve this material only by making it nano-crystalline when oxygen is introduced so that the bandgap becomes larger and a reduction of the absorption losses in the CdS layer is achieved.

**Table 2:** Parameters for CdTe and CdS films required for modeling

|  |  |  |
| --- | --- | --- |
| **Parameter** | **CdTe** | **CdS** |
| Thickness (μm) | 1-8 | 0.025 |
| Bandgap (eV) | 1.5 | 2.4 |
| Electron affinity (eV) | 3.9 | 4 |
| Dielectric permittivity (relative) | 9.4 | 10 |
| Electron mobility (cm2/V-s) | 500 | 350 |
| Hole mobility (cm2/V-s) | 60 | 50 |
| Electron thermal velocity (cm/s) | 1.00E+7 | 1.00E+7 |
| Hole thermal velocity (cm/s) | 1.00E+7 | 1.00E+7 |
| Electron density (cm-3) | - | 1.00E+15 |
| Hole density (cm-3) | 1.00E+17 | - |
| Light Intensity (W/cm2) | 0.1 | |

In Table 2, some important properties of CdTe and CdS thin films are shown as used while doing the simulation of CdS/CdTe solar cells. The donor concentration has been considered here as 1017 cm-3 but it strongly depends on the deposition method. We may expect better results for the open circuit voltage if this value is considered as 1 × 1018 cm-3 by some doping process. Electron diffusion length would be around 3–4 µm for these values. However, as reported in literature in the different laboratory conditions with diversified deposition techniques of CdTe this value may be approximated between 1 and 8 µm. The carrier concentration for majority carrier is also as low as 1 × 1015 cm-3. Increasing this value to 1016 cm-3 should also cause a higher built-in voltage.

**3.7 Variation of CdTe thickness:**

We need to check the impact of absorber layer thickness to the performance of the cell. As far as cost of the material is concerned we need make the layer thickness small but it may cause the degradation of cell performance.

**Table 3:** Performance values for different CdTe thickness values

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| CdTe(um) | CdS(nm) | Voc(V) | Isc(A) | FF(%) | η(%) |
| 0.5 | 35 | 0.7774 | 0.088 | 81.5438 | 11.157 |
| 0.8 | 35 | 0.7716 | 0.1034 | 84.2355 | 13.4412 |
| 1 | 35 | 0.7688 | 0.1106 | 82.7013 | 14.0641 |
| 1.5 | 35 | 0.7634 | 0.1234 | 84.5524 | 15.9303 |
| 2 | 35 | 0.7591 | 0.1319 | 83.5962 | 16.7402 |
| 2.5 | 35 | 0.7554 | 0.1382 | 81.8486 | 17.0894 |
| 3 | 35 | 0.7522 | 0.143 | 84.4595 | 18.1697 |
| 3.5 | 35 | 0.7493 | 0.1469 | 84.5602 | 18.6154 |
| 4 | 35 | 0.7467 | 0.1501 | 84.3869 | 18.9161 |
| 5 | 35 | 0.7422 | 0.1552 | 83.4243 | 19.2192 |
| 6 | 35 | 0.7385 | 0.159 | 82.4265 | 19.3573 |
| 7 | 35 | 0.7352 | 0.162 | 81.4971 | 19.413 |
| 8 | 35 | 0.7323 | 0.1644 | 84.4466 | 20.3331 |

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**Fig. 13:** I-V characteristics of CdTe/CdS solar cell with CdTe thickness 0.5 – 8 μm

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**Fig 14:** QE vs Wavelength curve of CdTe/CdS solar cell with CdTe thickness 0.5-8 micron

The dependencies of open-circuit voltage, efficiency, and fill factor of a CdS/CdTe solar cell have been checked to optimize these parameters and thus to improve the efficiency. The fill factor and open circuit voltage are controlled by of the forward current. The I-Vcharacteristic of the device which is originated primarily by recombination in the space charge region of the CdTe absorber layer is analyzed. From the I-Vcharacteristic of the solar cell it is well evident when the thickness of the absorber layer is increased it enhances the short circuit current and thus efficiency. Keeping the cost in mind we can’t go on increasing the thickness of the absorber layer\beyond a certain limit.

**3.8 Conclusion:**

The large drop off in device parameters along with decreasing thickness of the absorber suggests the cell performances are limited by optical issues as well as interface and back contact. Results may be improved by the addition of an acceptor defect between the window and absorber layer, especially when ultra thin absorbers are introduced, it creates the effect to increase in the interface defect density. Further for thinner cells the effect of the back contact needs to be investigated. CdTe–CdS device modeling needs around 50-100 parameters to obtain accurate results. The contribution of the interface for the thinner absorber layer restricts the device performance with the use of a limited parameter set.

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