

AN INTERLEAVED HIGH GAIN BOOST CONVERTER FOR RENEWABLE ENERGY APPLICATION

Abstract:

A new interleaved high gain boost converter is suggested for renewable energy application. By amalgamating coupled-inductor and switched capacitor boosting techniques, the suggested interleaved boost converter accomplishes very high step-up voltage gain unaccompanied by high turns ratio and extreme duty cycle. Though a classic DC-DC Boost converter can furnish a high output voltage with a smaller duty ratio, low efficiency and switch voltage stress are the shortcomings. Here in this interleaved boost converter by adopting the low-voltage rated switches and small RDS (On), the voltage stress of the switches is inferior than the output voltage. Also the efficiency of the converter have heightened. Thus two drawbacks of classic boost converter is eliminated here. The experimental results, using a prototype of 18V/400V, corroborate the efficacious performance of suggested converter.

Keywords: Coupled inductor, High gain boost converter, Interleaved, Switched capacitor.

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I. INTRODUCTION

In electrical and electronics engineering, power electronics associates with the processing of high voltages and currents to deliver power that aids a variety of needs. Over the last few years, need to power electronic equipment has elevated tremendously. Another interesting fact is that the consciousness towards renewable energy sources (eg: Solar energy) also heightened due to the environmental problems prompted by fossil fuels and global warming. The main snag of these power sources is that they lack the potentiality to generate high DC voltage. For that reason the need to use the power electronic equipment (ie: Power electronic converters) has maximized more than before. Together with escalating growth of renewable power, the power electronic converters have also undergone changes in structure and design to increase performance and efficiency. Long ago a traditional DC-DC boost converter were used as power electronic converters in photovoltaic (PV) systems. The prime merit of this typical boost converter is that its simple structure. Their elevated voltage stress, low power density, reverse recovery problem, output voltage sensitivity to the duty cycle and high current ripple are the stumbling blocks. The DC voltage in step-up DC-DC converter increases mainly by storing energy at the input side and releasing it towards the output [1]. Fundamentally, such converters are divided into non isolated and isolated types [2]. The fly-back converters [4]-[5] and the forward converters [6]-[7] are examples of this categorization. The non isolated converters are unification of conventional DC-DC converter and voltage boosting techniques. The switched capacitors [8]-[11], the switched inductors [12]-[14], the voltage multipliers [15], the coupled inductors [16]-[19] and multiphase converter topology (ie: Interleaved) are among the preeminent voltage boosting methods. When coupled inductors are used, the main advantage is that the number of magnetic cores will definitely decrease. Switched inductor and switched capacitors boosting techniques are the combination of diodes- inductors and diodes-capacitors respectively. At the present time, the prime focus of researchers are on mitigating the problems arose by expanding the voltage gain in newer converter topologies. The predicaments of these topologies are voltage stress of semiconductors, lower efficiency, current ripple, lack of soft-switching conditions. The voltage boosting techniques switched capacitor/switched coupled inductors are described detail in [20]. Here in this converter the magnitude of stress arose is low. In [21] a high boost Dc-Dc converter structure composed of switched capacitors and coupled inductors is introduced and explained. The main defect of this converter is that the vulnerability of its voltage gain towards duty cycle.

This chapter suggests a novel high gain boost converter in the company of an interleaved structure and a network comprising of coupled inductors and switched capacitor cells. The chief contributions of this study are,

- (i)The voltage conversion ratio get increased.
- (ii)The converter have very low switch voltage stress.
- (iii)It has high efficiency.
- (iv)Its input current ripple is remarkably diminished.

II. PROPOSED CONVERTER STRUCTURE

Figure 1 shows a two phase interleaved boost converter [24]. Its circuit components are grouped into three stages. Its input stage comprised of two coupled inductors and two power switches (S1 and S2). In the middle stage, it has five capacitors (C1-C5) and six diodes (D1-

D6) as energy transfer. Finally, the output stage contain the output capacitor (C_o) and the load (R). In order to accomplish ultra high voltage gain, two sets of switched capacitor networks were placed back to back. Figure 2 illustrates the equivalent circuit of the suggested structure. The adopted duty cycle ratio is 0.55. Here the proposed converter has principally four operation modes.

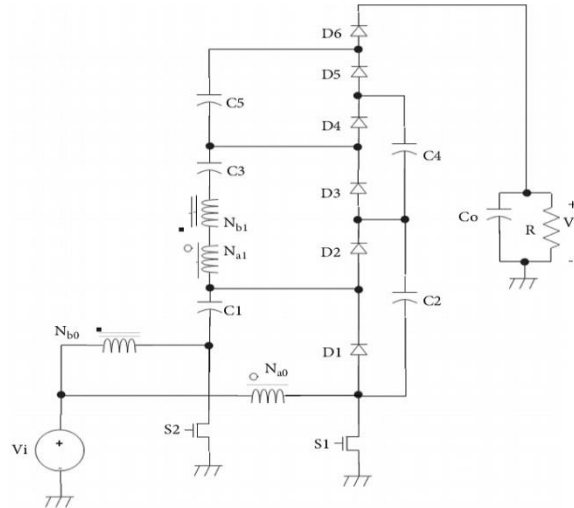


Figure 1: Power circuit of interleaved boost converter

A. Operation Principles

Consider the following assumptions:

- (1) The circuit components employed are *ideal*.
- (2) *Large capacitors* are used.

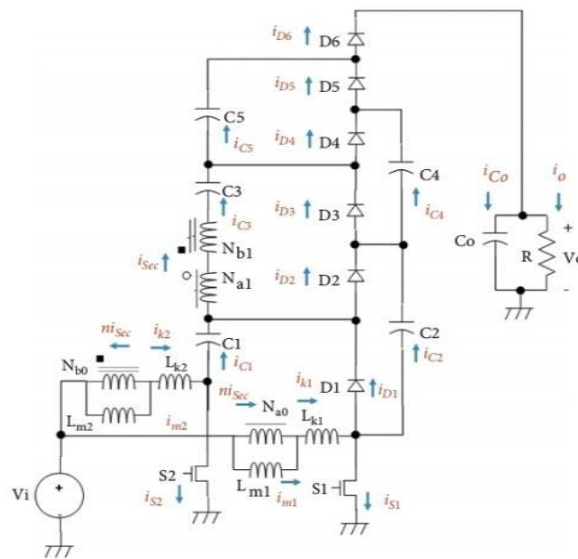


Figure 2: Equivalent circuit

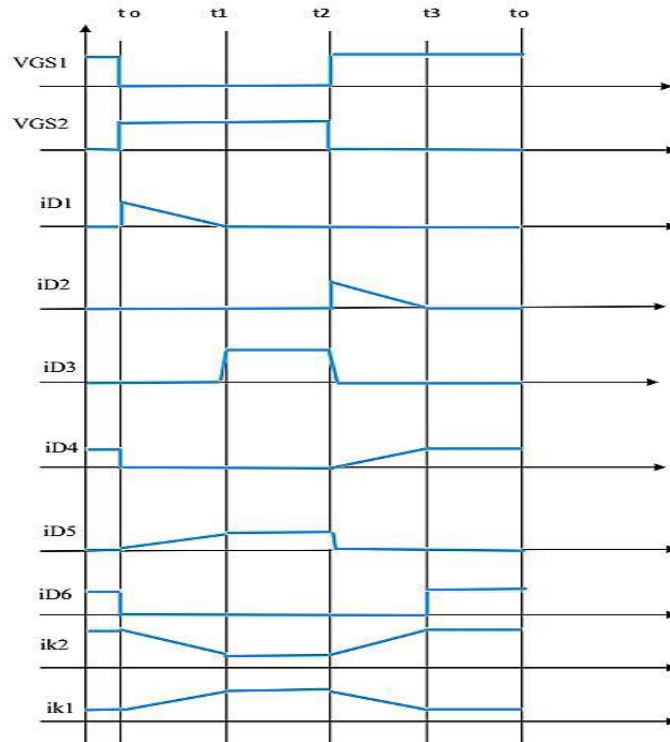


Figure 3: Key waveforms in CCM operation

1) **Mode 1 [t₀-t₁]**: At t₀, S₁ is turned off. D₁ and D₅ conduct. L_{k2} and L_{m2} are charged through the input. The leakage current i_{k1}, charges C₁ and other capacitors are swapping energy. i_{D1} is decreased.

$$V_{m1} = V_i - V_{C1} \quad (1)$$

$$V_{m2} = V_i \quad (2)$$

2) **Mode 2 [t₁-t₂]**: i_{D1} decreases linearly in the previous mode. This current turns into zilch at t₁ and D₁ turns off naturally according to Figure 4(b). In this mode D₃ starts to conduct.

$$V_i = V_{C1} - V_{C2} + V_{C3} - n(V_{m2} - V_{m1}) + V_{m1}$$

$$V_{m2} = V_i \quad (3)$$

3) **Mode 3 [t₂-t₃]**: S₂ is turned off at t₂ as shown in Figure 4(c). D₂ and D₄ conduct. L_{k1} and L_{m1} are get charged. Here C₃ act as a voltage source. i_{D2} is decreased. Thus C₂ is charged.

$$V_{m1} = V_i \quad (4)$$

$$V_{m2} = V_i + V_{C1} - V_{C2} \quad (5)$$

4) **Mode 4 [t₃-t₀]**: i_{D2} becomes zero at t₃. D₂ is turned off naturally according to Figure 4(d). In this mode D₆ starts to conduct.

$$V_i = V_o + V_{m2} - V_{C1} - V_{C3} - V_{C5} - n(V_{m1} - V_{m2}) \quad (6)$$

III. STEADY-STATE ANALYSIS

A. Voltage Gain: By applying *volt-second balance principle*, the following equations are expressed:

$$V_{m1}^{on} D T + V_{m1}^{off} (1 - D) T = 0$$

$$V_i D T + (V_i - V_{C1}) (1 - D) T = 0 \quad (7)$$

Here D and T implies duty cycle ratio and switching period respectively. From equation (15), the voltage of C1 earned is,

$$V_{C1} = \frac{1}{(1-D)} V_i \quad (8)$$

Using (16) and (17), the voltage obtained for C2 is,

$$V_{C2} = \frac{2}{(1-D)} V_i \quad (9)$$

Using equations (1)–(18), the voltage of C3 is,

$$V_{C3} = \frac{n+2}{(1-D)} V_i \quad (10)$$

Using equations (6)–(8) and (13) to (14), the voltage of C4 is obtained as follows:

$$V_{C4} = \frac{2n+2}{(1-D)} V_i \quad (11)$$

Thus, using (7),

$$V_{C5} = \frac{2n+2}{(1-D)} V_i \quad (12)$$

Using equations (11), (13), (17), (18), (19) and (21), the voltage gain earned is,

$$M = \frac{V_o}{V_i} = \frac{(4n+6)}{(1-D)} \quad (13)$$

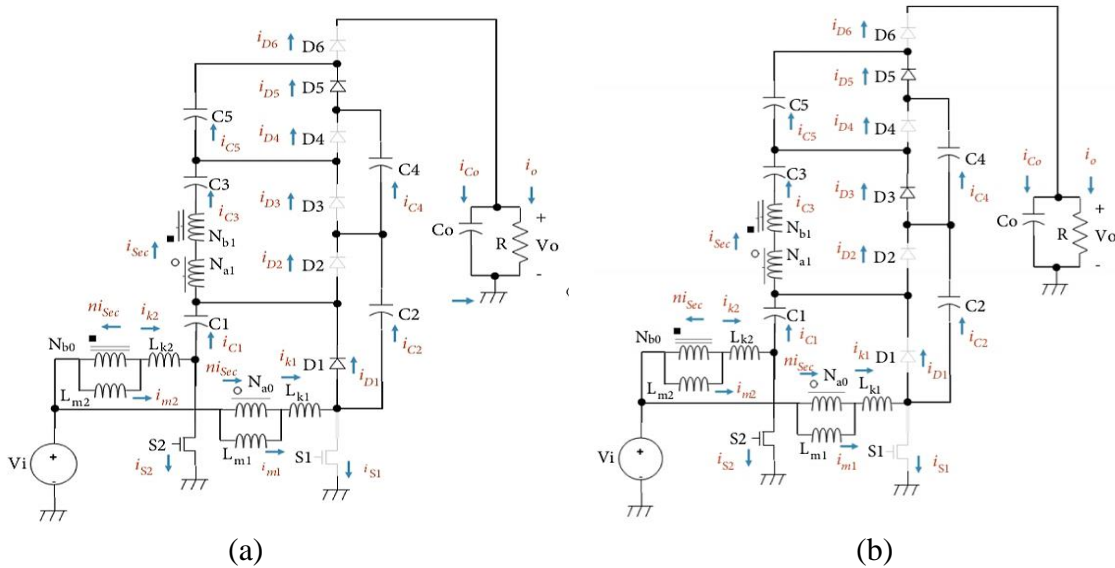
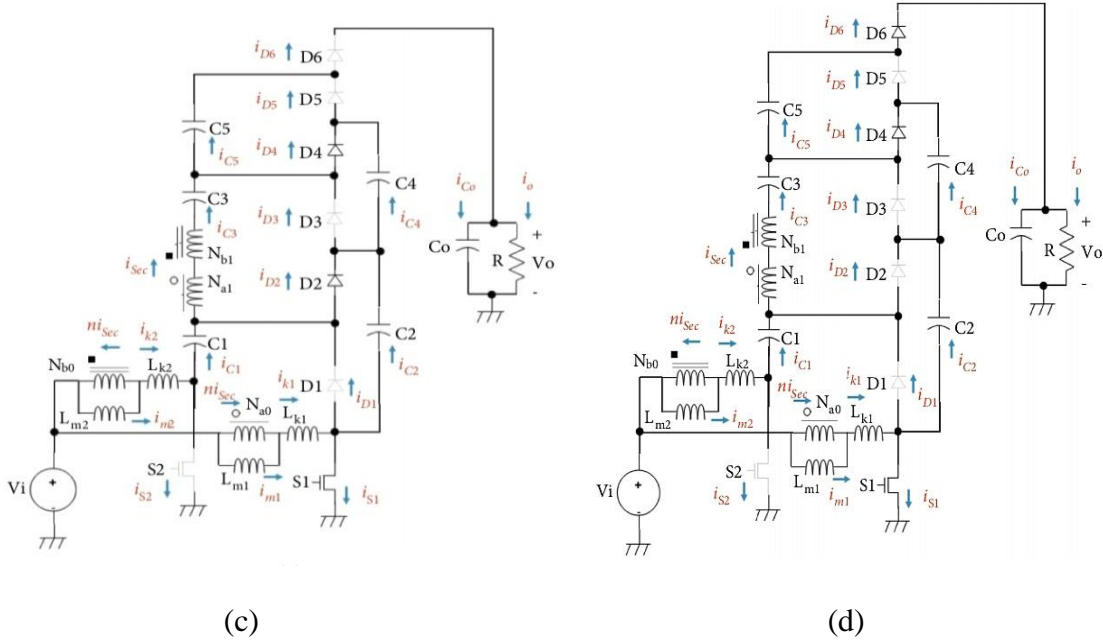


Figure 4: Circuits corresponding to the operation modes: (a) mode 1 [t0-t1]; (b) mode 2 [t1-t2]; (c) mode 3 [t2-t3]; (d) mode 4 [t3-t0].



B. Voltage Stress: For capacitors, the equations of voltage stress are,

$$V_{C1} = \frac{1}{4n + 6} V_o$$

$$V_{C2} = \frac{2}{(4n+6)} V_o \quad (14)$$

$$V_{C3} = \frac{n + 2}{4n + 6} V_o$$

$$V_{C4} = V_{C5} = \frac{2n + 2}{4n + 6} V_o$$

The voltage stress of the switches are,

$$\begin{aligned} V_{S1} &= V_{S2} \\ &= \frac{1}{1-D} V_i \\ &= \frac{1}{4n+6} V_o \quad (15) \end{aligned}$$

Hence when n=1, voltage stress equations are one-tenth of the output voltage (ie: conduction losses in the proposed converter are decreased with a small $R_{DS(on)}$).

For diodes, the voltage stress equations are,

$$\begin{aligned} V_{D1} &= V_{D2} \\ &= | -V_{C2} | \\ &= \frac{2}{4n+6} V_o \end{aligned}$$

$$\begin{aligned}
 V_{D3} &= V_{D4} \\
 &= | -V_{C4} | \\
 &= \frac{2n+2}{4n+6} V_o \quad (16) \\
 V_{D6} &= |V_{C1} + V_{C3} + V_{C5} + V_o | \\
 &= \frac{n+1}{4n+6} V_o
 \end{aligned}$$

C. Input Current Ripple and magnetizing Inductance: Here the current gain is,

$$\frac{I_o}{I_i} \langle \text{Avg} \rangle = \frac{1-D}{4n+6} \quad (17)$$

Let I_{m1_Avg} and I_{m2_Avg} are average magnetizing currents, then they are narrated by the following equation with the support of the equation (26),

$$\begin{aligned}
 I_{m1_Avg} &= I_{m2_Avg} \\
 &= I_m _ Avg \\
 &= \frac{I_i _ Avg}{2} \quad (18) \\
 &= \frac{2n+3}{(1-D)} I_o _ Avg
 \end{aligned}$$

The input current is,

$$\begin{aligned}
 i_i &= (i_{m1} + ni_{sec}) + (i_{m2} - ni_{sec}) \\
 &= i_{m1} + i_{m2} \quad (19)
 \end{aligned}$$

The ripple of the input and magnetizing currents is,

$$\Delta i_m = \frac{D}{L_m f_s} V_i \quad (20)$$

$$\Delta i_i = \frac{2D-1}{L_m f_s} V_i \quad (21)$$

IV. THE DESIGN OF CONVERTER COMPONENTS

A. Coupled Inductors: Select a duty ratio cycle (D) greater than 0.5. Here the turns ratio is,

$$n = \frac{M(1-D)-6}{4} \quad (22)$$

The magnetizing inductances are,

$$\begin{aligned}
 L_{m1} &= L_{m2} \\
 &= L_m \\
 &= \frac{D.V_i}{\Delta i_m f_s} \quad (23)
 \end{aligned}$$

Prime condition should be satisfied is that $I_m _ Avg > \left(\frac{1}{2}\right) \Delta i_m$. Thus, the minimum magnetizing inductance is,

$$L_m > \frac{1}{2} \frac{(1-D)D.V_i}{(2n+3)I_o _ Avg f_s} \quad (24)$$

The leakage inductance are,

$$\begin{aligned}
 L_{k1} &= L_{k2} \\
 &= L_k \quad (25)
 \end{aligned}$$

$$= \frac{(n+1)V_o}{4(2n+3)x}, \frac{diD3(t)}{dt} = x$$

Considering (27) and (29), peak magnetizing currents are gained as follows,

$$\begin{aligned} I_{m1_Pk} &= I_{m2_Pk} \\ &= I_{m_Pk} \\ &= \frac{2n+3}{(1-D)} I_{o_Avg} + \frac{1}{2} \frac{D.V_i}{L_{mfs}} \end{aligned} \quad (26)$$

B. Semiconductors: Average current of all diodes is,

$$I_{D1_Avg}, \dots, I_{D6_Avg} = I_o \text{ Avg.} \quad (27)$$

According to equation (38), the diode's peak current are earned by arranging the equation (37) as follows:

$$I_o \text{ Avg} = \frac{1}{2} (I_{D1_Pk} \dots I_{D6_Pk})(1 - D) \quad (28)$$

$$I_{D1_Pk} \dots I_{D6_Pk} = \frac{2.I_o_Avg}{(1-D)} \quad (29)$$

The peak current of the power switches are,

$$\begin{aligned} I_{S1_Pk} &\approx \frac{i_{i_Avg}}{2} + I_{D2_Pk} + nI_{D4_Pk} = \frac{(4n+5)I_o_Avg}{(1-D)} \\ I_{S2_Pk} &\approx \frac{i_{i_Avg}}{2} + nI_{D3_Pk} + nI_{D5_Pk} = \frac{(6n+3)I_o_Avg}{(1-D)} \end{aligned} \quad (30)$$

By the equation (27) and considering the operating modes the RMS current of the switches are,

$$I_{S1_RMS} = \frac{(2n+3)I_o_Avg}{(1-D)} \left(\sqrt{(1-2D) - \frac{4(1-D)(n^3 + 3n^2 + 3n + 1)}{n^3 + 4n^2 + 5n + 2}} \right) \quad (31)$$

$$I_{S2_RMS} = \frac{(2n+3)I_o_Avg}{(1-D)} \left(\sqrt{3 - 2D} \right) \quad (32)$$

C.Capacitors: The design equations of capacitors are,

$$C1 = \frac{4n+6}{\Delta V_c V_o^2 f_s}$$

$$C2 = \frac{(2n+3)P_o}{\Delta V_c V_o^2 f_s}$$

$$C3 = \frac{(4n+6)P_o}{(n+2)\Delta V_c V_o^2 f_s}$$

$$C4 = C5 = \frac{(2n+3)P_o}{(n+1)\Delta V_c V_o^2 f_s} \quad (33)$$

V. COMPARISON

Table 1 compares the suggested converter with other converters that are similar in topology and structure. The number of switches and number of magnetic cores used in suggested converter are same as that of the converters in [24] and [25]. Also the efficiency get increased in this converter by 96.6%.

Table 1: Comparison of the suggested converter with similar converters

Topologies	Voltage gain	S	D	C	M	Efficiency (%)
[24]	$\frac{(2N + 4)}{(1 - D)}$	2	4	4	2	94.9
[25]	$\frac{(4N + 4)}{(1 - D)}$	2	4	4	2	94.5
Proposed	$\frac{(4N + 6)}{(1 - D)}$	2	6	6	2	96.6

S – No. of power switches; D – No. of diodes;
 C – No. of capacitors; M – No. of magnetic cores.

VI. SIMULATION RESULTS

The suggested system was simulated in MATLAB/Simulink. Table 2 shows the simulation design parameters and its values. The magnetizing and leakage inductances are $100\mu\text{H}$ and $2.5\mu\text{H}$ respectively. The capacitors used are 20, 10, 7, 5, 5 and $2*56\mu\text{F}$. The duty cycle ratio (D) is 0.55.

Figure 5 and Figure 6 shows the output voltage obtained from this interleaved boost converter (V_{out}) and the waveform of gate pulses of the switches S1 and S2. The **output voltage** obtained from this converter is **22.22** times the **input voltage**.

Table 2: Simulation parameters

No.	Parameters	Values
1	Input voltage	18V
2	Output voltage	400V
3	Magnetizing and Leakage inductances (L_m and L_k)	$100\mu\text{H}$ and $2.5\mu\text{H}$
4	Capacitors	20, 10, 7, 5, 5 and $2*56\mu\text{F}$
5	Turns ratio	1:1

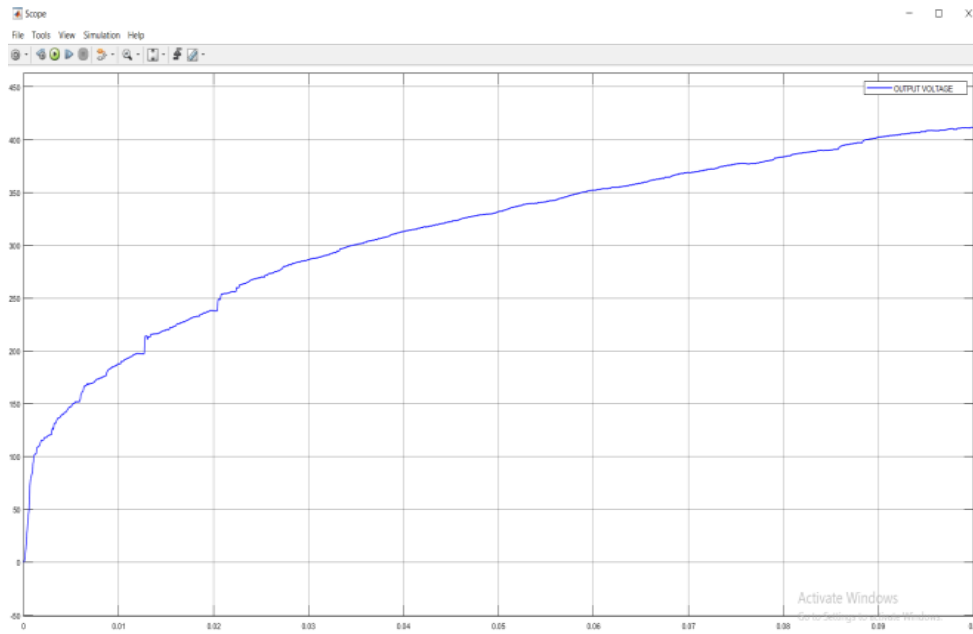


Figure 5: Output voltage obtained from the simulation circuit

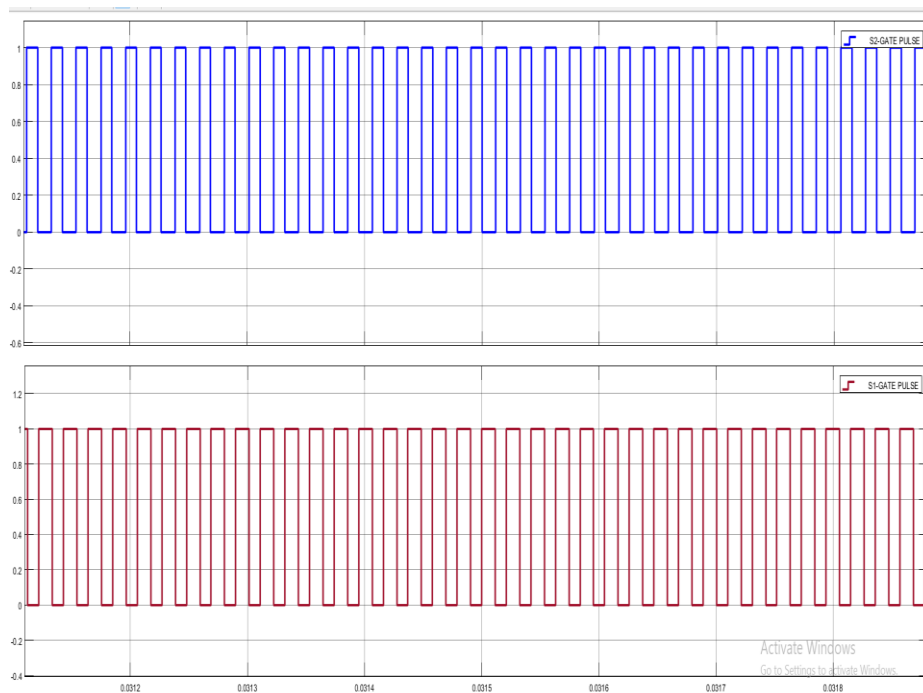


Figure 6: Gate pulses

VII. EXPERIMENTAL RESULTS

A 18V/400V interleaved boost converter was constructed. The main specifications of the prototype is given in Table 3. The sampling time is 21 microseconds. Value of n taken for coupled inductors are 1 and each winding comprises of 32 number of turns. MOSFETs

employed are **IPB072N15N3G** and Schottky diodes (**MBR40250** and **MBR20150**) are utilized to implement the prototype of suggested converter. The duty cycle is 0.55. The measured maximum efficiency of the converter is 96.6%.

Table 3: Specifications

Parameters	Description
Input voltage, V_i	18 V
Output voltage, V_o	400 V
Switching frequency, f_s	47kHz
Capacitors(C_1, C_2, C_3, C_4, C_5 and C_o)	5, 5, 7, 20, 10 and $2 \times 56 \mu\text{F}$
Inductances (L_m and L_k)	$100 \mu\text{H}$ and $2.5 \mu\text{H}$
Turns ratio	1:1
Diodes(D_3, D_4 and D_5)	MBR40250
Diodes(D_1, D_2 and D_6)	MBR20150
Power switches (S_1 and S_2)	IPB072N15N3G

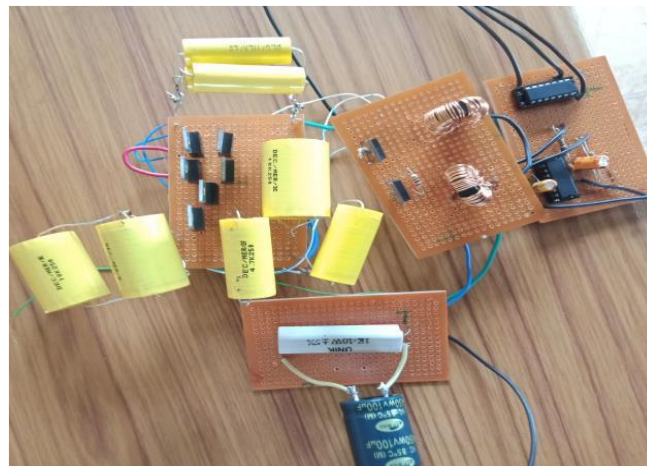


Figure 7: Experimental set-up

VIII. CONCLUSION

The suggested interleaved boost converter is a unification of two coupled inductors and switched capacitor boosting techniques. Its benefits are high voltage gain, high efficiency (96.6%), conduction loss is low in magnitude due to the use of advanced power switches and low converter loss. The results obtained from simulation circuit and prototype unveiled the efficacy of the suggested interleaved boost converter.

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